90 Series μP BOARD TESTER

USER'S MANUAL

FLUKE AND PHILIPS
THE T&M ALLIANCE

FLUKE

LIMITED WARRANTY

Fluke warrants the 90 Series to be free from defects in material and workmanship under normal use and service for 1 year from the date of shipment. This warranty extends to you if you are the original purchaser and does not apply to fuses, batteries, or any product which, in our sole opinion, has been subject to misuse, alteration, or abnormal conditions of operation or handling.

To obtain warranty service, contact a Fluke Service Center or send the product, with a description of the difficulty, postage and insurance prepaid, to the nearest Fluke Service Center. We assume no risk for damage in transit.

We will, at our option, repair or replace the defective product free of charge or refund your purchase price. However, if we determine that the failure was caused by misuse, alteration, or abnormal condition of operation, or handling, you will be billed for the repair. The repaired product will be returned to you, transportation prepaid.

THIS WARRANTY IS EXCLUSIVE AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITIED TO ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR USE. FLUKE WILL NOT BE LIABLE FOR ANY SPECIAL, INDIRECT, INCIDENTAL, OR CONSEQUENTIAL DAMAGES OF LOSS WHETHER IN CONTRACT, TORT, OR OTHERWISE.

90 Series

µP BOARD TESTER

User's Manual

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February 1988

FLUKE

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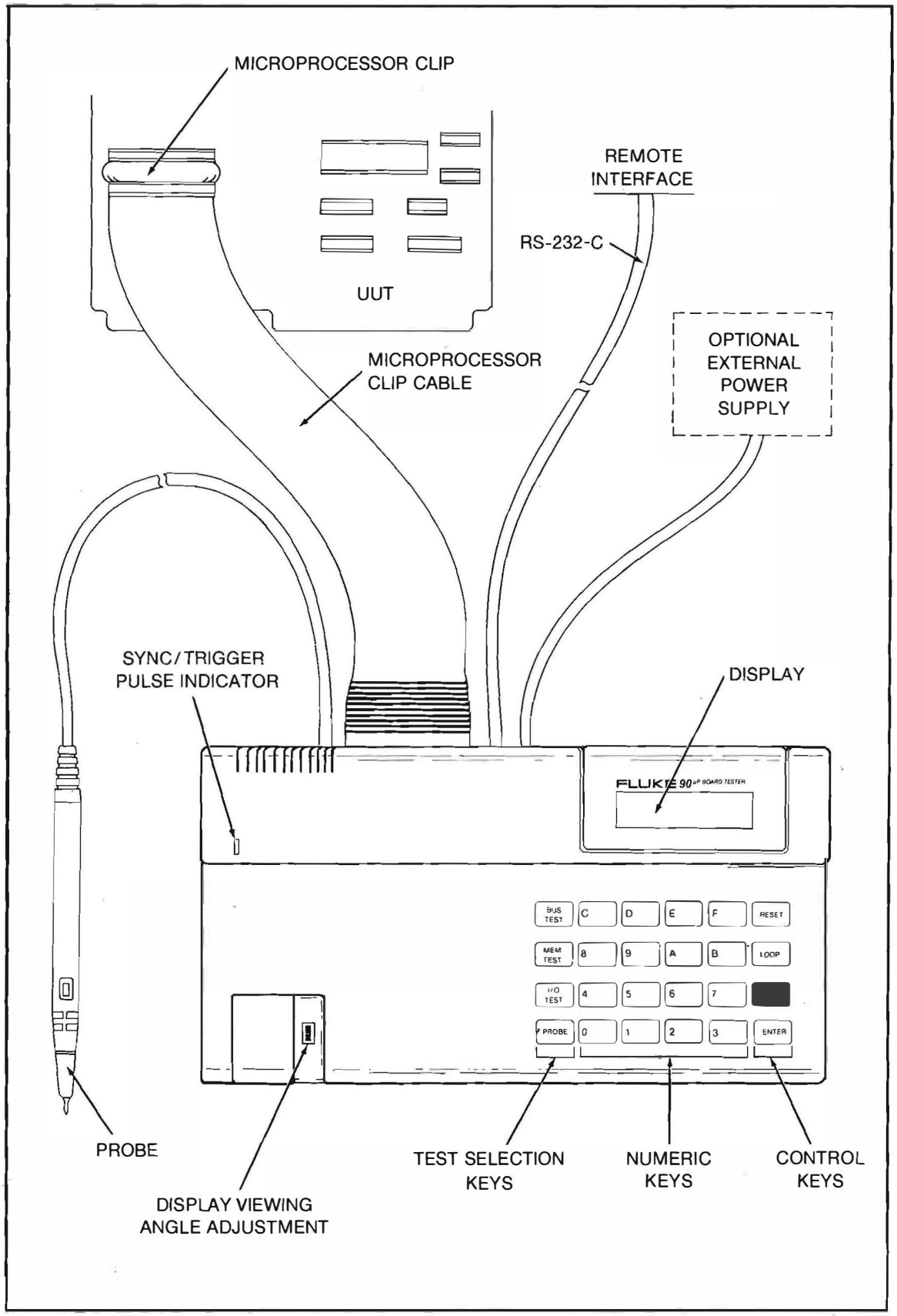


90 Series µP Board Tester System

Section 1
Introduction

GENERAL DESCRIPTION

The Fluke 90 μP Board Tester (also referred to as "the tester") is a hand-held, easy-to-operate, tester used to diagnose faults in microprocessor-based devices. The tester is a Direct Memory Access (DMA) device emulator that connects to the microprocessor in the UUT (unit under test). The microprocessor does not have to be removed from the circuit. The tester forces the DMA and WAIT lines on the UUT bus, taking control of the bus from the UUT's microprocessor.

Power is supplied by either the +5 volt line at the UUT microprocessor or by an (optional) external power supply. No connection is required to the UUT other than the microprocessor clip. Refer to Section 2 for more information on the external power supply.

The Fluke 90 performs the following:

- Bus Tests to determine if any bus line is stuck high or low, or shorted to other bus lines.
- Memory Tests to determine if RAM can be written and read and if ROM contains the proper bit pattern.
- I/O Tests to determine if I/O addresses can be written and read.
- QuickTrace™ to identify the signal name of an address, data, or control signal line and allows the type of signal line to be tracked in the UUT.
- Detect selected events on the UUT bus by setting and enabling Break-Point, Frame-Point, and SYNC/Trigger Interface functions.
- Loads the UUT memory over the Remote Communications Interface.
- Dumps the contents of the UUT memory to a remote terminal or computer via the Remote Communications Interface.

To use the tester effectively, you should have a solid background of digital electronics and basic microprocessor architecture.

* QuickTrace is a Trademark of John Fluke Mfg. Co., Inc. Everett, Washington.

OPERATING PRECONDITIONS

The tester can be used only under the following circumstances:

- The tester forces the DMA control line(s) on the bus. For proper operation, these control lines must not be tied directly to the power supply (Vcc) or ground. The DMA control line(s) cannot be bussed together or bussed to any other control line(s). If this situation exits, refer to the introduction of Section 3 for possible remedies.

- Power must be supplied to the microprocessor in the UUT. If the tester is powered by the optional external power supply, the UUT microprocessor must still be powered. This is done to prevent the tester from supplying power to the UUT.

- Each tester model is microprocessor-specific; that is, it can be used on only one type of microprocessor.

FLUKE 90/UUT FLOATING-GROUND HAZARD

WARNING

TO AVOID ELECTRICAL SHOCK, ENSURE THAT THE MAXIMUM VOLTAGE FROM THE UUT DOES NOT EXCEED 30V ABOVE EARTH GROUND.

To determine if the UUT ground is floating, take a voltmeter and measure the voltage between the UUT ground and a known good earth ground. If you are using a computer to control the tester, a potential floating-ground hazard may exist. There is usually no isolation between the computer and the RS-232-C interface, the tester and UUT ground. Check the voltage potential between the earth ground of the remote computer and the UUT ground. If there is a voltage measurement (>1V), a large current may flow through the tester and cause damage.

THE FLUKE 90 USER'S MANUAL

The User's Manual provides general operating information and is not specific to the microprocessor your tester supports. Refer to the decal on the bottom of the tester for specific operating information concerning the microprocessor of the UUT.

Section 2
Features and Functions

INTRODUCTION

Section 2 describes the general layout and operating features of the tester. Refer to Figure 2-1 for the top panel view and Figure 2-2 for the rear panel view.

UNPACKING THE TESTER

Remove the packing material and tester from the shipping container. The tester is shipped with the Probe, an RS-232-C cable, a cable adapter, and this manual. Save the shipping container and packing material in case you have to reship the tester.

Check the shipment carefully. If anything is missing or damaged, contact the place of purchase immediately. If reshipment is necessary, use the original shipping container and packing material. If the original container is not available, be sure that adequate protection is provided to ensure that the tester is not damaged in transit.

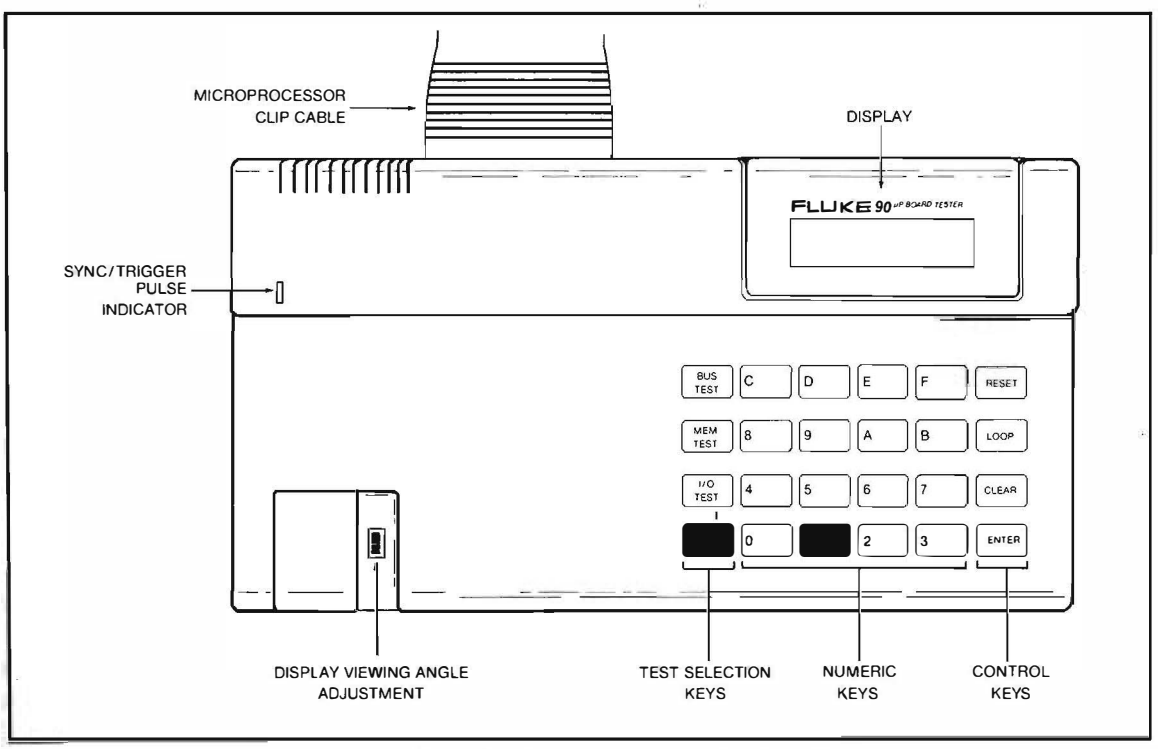


Figure 2-1. Case Top Feature and Function Locations

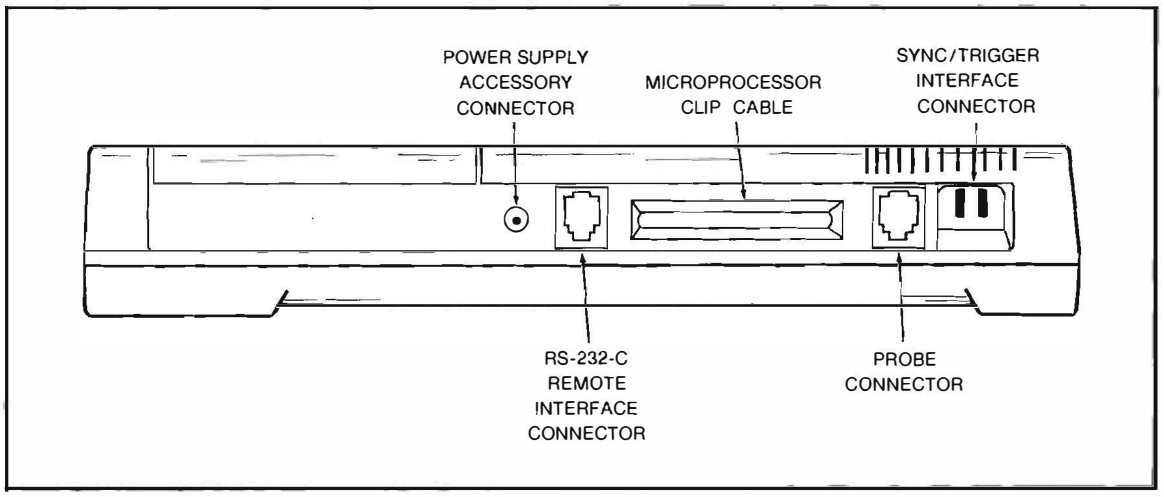


Figure 2-2. Rear Panel Feature and Function Locations

THE DISPLAY

The display, (refer to Figure 2-1 for location), is a two line, 16-character per line, liquid crystal panel. The right-most character in the bottom line is reserved for an activity indicator. The indicator flashes light to dark when the tester is executing a test.

DISPLAY VIEWING ANGLE ADJUSTMENT

The Display Viewing Angle Adjustment is a thumbwheel control that adjusts the display contrast. Refer to Figure 2-1 for its location. Rotate the control in either direction for improved contrast of the display at various viewing angles.

KEYPAD

The keypad, (shown in Figure 2-3), consists of 24 keys arranged in a four-high by six-wide matrix. The keys are used to select, execute, and stop tests, and also enter addresses and data.

Test Keys

Four test keys (BUS TEST, MEM[ory] TEST, I/O TEST, AND PROBE) are located along the left side of the keypad. Each key corresponds to a test category. Refer to Section 3 for a more detailed explanation of each key.

A menu of tests is associated with each test key. To access the menu, press a test key. The last test performed is displayed. Press the test key repeatedly to scroll through available tests until the name of the test you desire is displayed. Refer to Table 2-1 for the tests available on each test key.

Control Keys

Four control keys (RESET, LOOP, CLEAR, and ENTER) are located along the right edge of the keypad. These keys are used with the test keys and numeric keys (discussed below) to control the various operations of the the tester. A general description of each control key is provided below. For additional information pertaining to the operation of a key in a particular test, refer to the discussion of that test in Section 3.

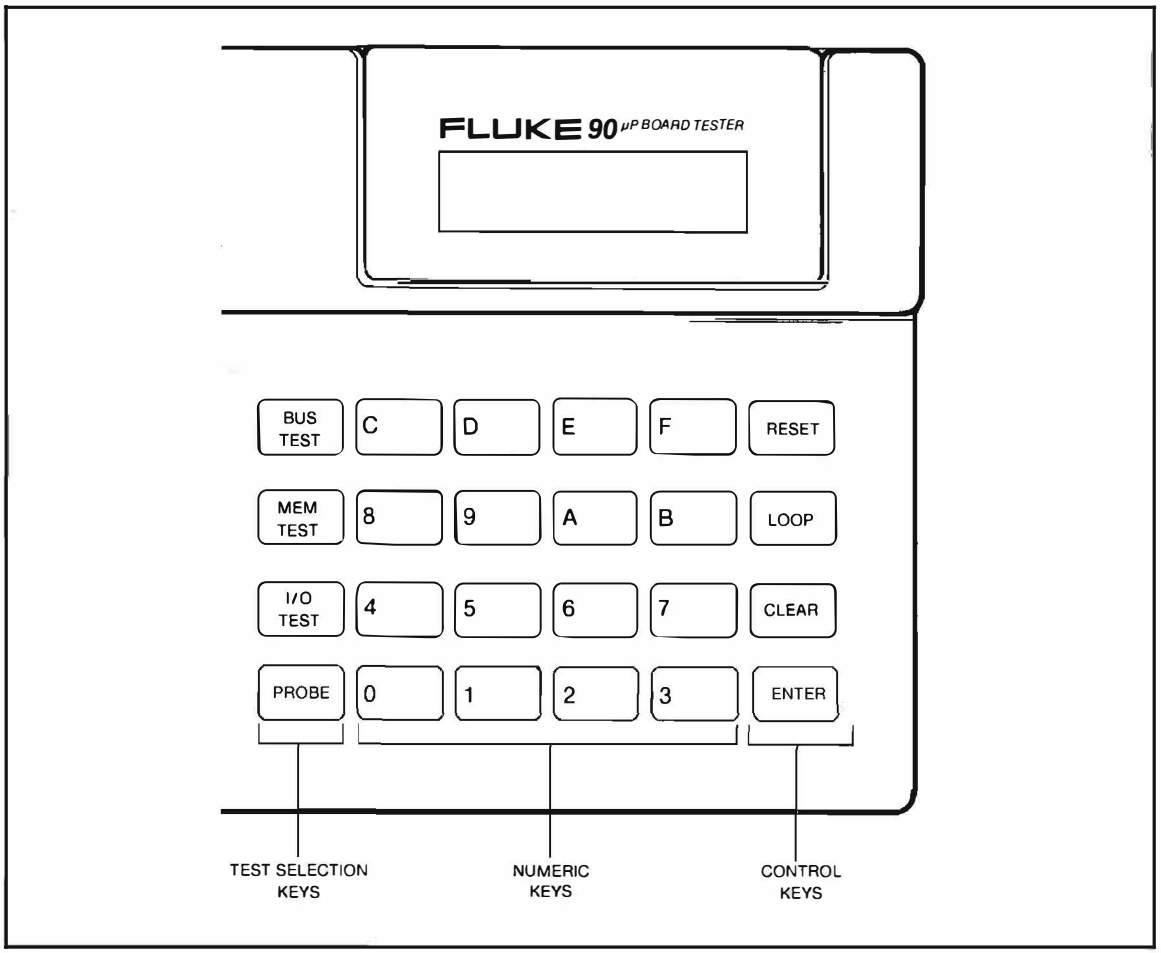


Figure 2-3. Keypad

- RESET Key

  Press the RESET key to reset the operation of both the UUT and the tester. The RESET key can also be used to exit from any test or function in addition to the tester and the UUT being reset.

- LOOP Key

  Press the LOOP key to enter a looping mode on the Bus, Memory, and I/O tests. Looping causes a test to be repeated until the RESET key or CLEAR key is pressed. In the looping mode, the activity indicator on the bottom line of the display flashes.

NOTE

Use the CLEAR key rather than the RESET key to stop the looping mode. The CLEAR key resets the tester only; it does not reset the UUT. The RESET key resets the UUT microprocessor as well as the tester, which in some cases is an undesirable situation.

In the RS-232-C Port Configuration Mode (discussed in Section 3), the LOOP key is used to select baud rate and character length. In the Probe Address, Data, and Control modes, the LOOP key is used to backup to the previous probed signal.

Table 2-1. Test Keys Menu Listing

TEST KEY	MENU SELECTIONS
Bus Test	Test Bus Ramp Test Shift Test
Mem[ory] Test	Test Memory Checksum Test Memory Examine Memory Verify Memory Write Memory Soak
I/O Test	I/O Examine * I/O Verify * I/O Write * RS-232-C Port Configuration
Probe	QuickTrace Probe Address Probe Data Probe Control

* Only for Microprocessors with I/O ports.

- CLEAR Key

  Press the CLEAR key once to clear address or data entries in progress. For example, if an address is being entered and an error is made, a single depression of the CLEAR key clears the digits already entered and changes all the digit display spaces to "?" marks.

  Press the CLEAR Key a second time to abort a partially completed data entry. For example, if you enter the data for a memory write test, pressing the CLEAR key twice cancels data entry and allows you to select a different test.

  If a test or Probe function is executing, a single push of the CLEAR key causes termination of the test or function.

- ENTER Key

  Press the ENTER Key to execute the test indicated on the display, or complete the entry of data or an address. The push button on the Probe performs the same function as the ENTER key on the keypad. For more information on the Probe ENTER button, see Section 3 "Using the Probe".

NOTE

In the Remote Mode, only the CLEAR and RESET keys are active.

Numeric Keys

The Numeric keys (0 to F), located in the middle of the keypad, are used to enter hexadecimal values needed for the type of test being performed.

MICROPROCESSOR CLIP AND CABLE

The microprocessor cable with attached clip supports only one type of microprocessor family. Information on the bottom of the tester states which microprocessor your tester supports. The spring-loaded clip is detachable from the cable. The cable is not detachable from the tester without opening the case.

CAUTION

Do not use the microprocessor cable as a handle to carry the tester. Damage may occur to the connection between the cable and the circuit board.

PROBE AND PROBE CONNECTOR

The Probe, (shown in Figure 2-4), is a hand-held device that detects signal states on the UUT. The Probe operates in specific capacities during the Probe Address, Data, Control, and QuickTrace functions. These functions are described in Section 3 of this manual. When these functions are not active, the Probe lights indicate the states of UUT signals. The Probe plugs into a connector located on the rear panel of the tester. (See Figure 2-2 for the location of the connector.)

If the signal being probed is in the high state (or the Probe is not touching a valid digital signal), the red light on the Probe is lit. If the signal is in the low state, the green light is lit. If the signal is toggling between a high and low state, both red and green lights flash rapidly at a rate that depends on the frequency of the signal (the higher the frequency, the higher the flash rate). During Memory and I/O tests, the Probe is synchronized to the rising edge of the data valid state on the UUT bus. For all tester controlled read/write cycles refer to the Probe timing diagram Figure 2-5. Whenever the tester is not executing a test, the Probe is synchronized to the rising edge of the data valid state on the UUT bus for all UUT read/write cycles.

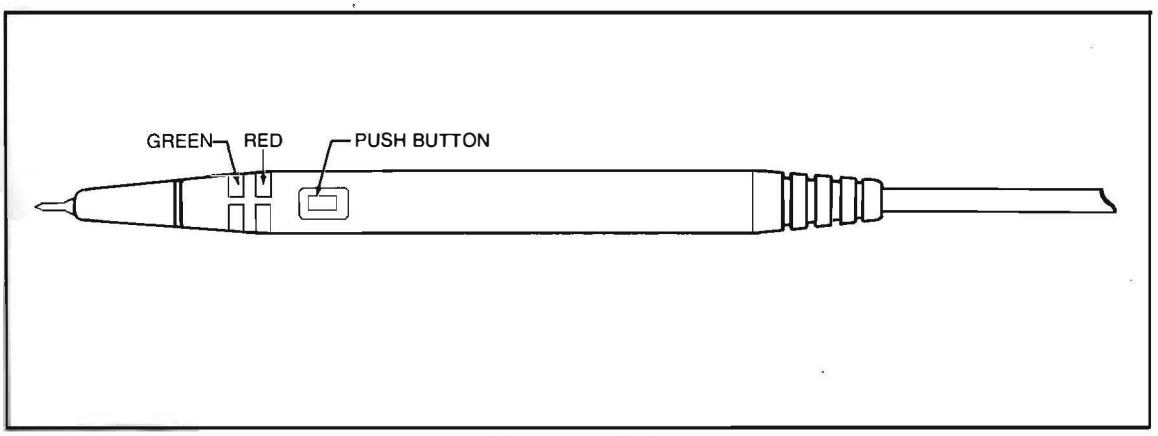


Figure 2-4. Probe

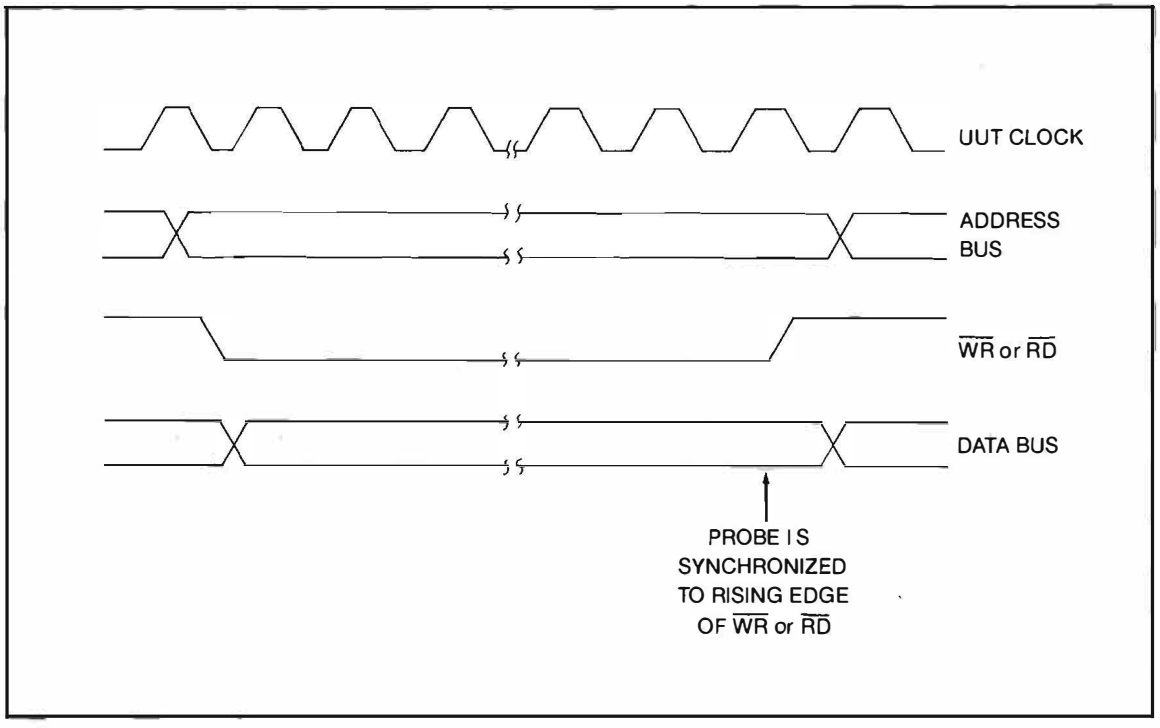


Figure 2-5. Probe Timing Wave Form

REMOTE INTERFACE CONNECTOR

The tester is provided with an RS-232-C Interface connector for remote communication with a host computer or terminal. The RS-232-C Remote Interface connector is located on the rear panel of the tester. (See Figure 2-2.)

All tests and Probe functions that can be executed at the keypad can also be executed over the Remote Interface. Additional tests can be executed over the Remote Interface only. A more detailed description of the Remote Interface commands and additional tests are located in Section 4 of this manual. Refer to Section 4 for the pinout of the back panel connector.

EXTERNAL POWER SUPPLY

The External Power Supply is an accessory that provides operating power to the tester. In some cases, the UUT power supply may not be able to support its own needs and also supply power to the tester. If UUT +5 voltage supply falls below 4.35V dc, the tester display remains blank.

The External Power Supply is a 7 to 12 volt unregulated DC Supply with 0.2 Amp minimum and 0.5 Amp maximum capacity. It plugs into the rear panel of the tester (see Figure 2-2). The outputs must be isolated from the line. The plug used is a subminiture phone plug shown in Figure 2-6.

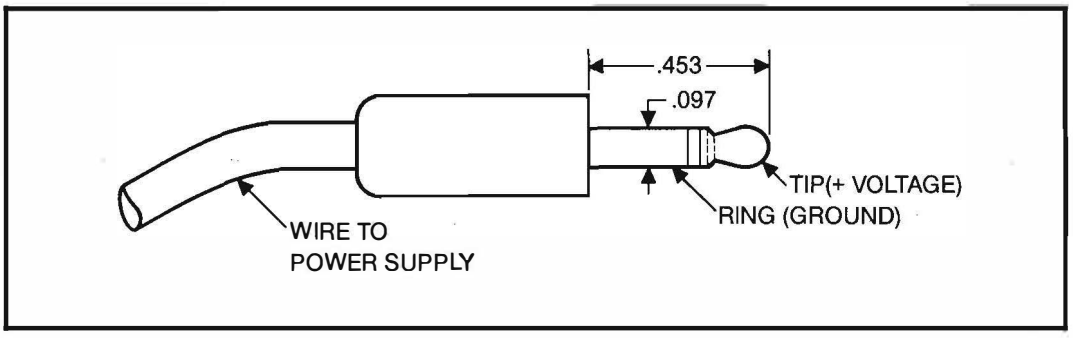


Figure 2-6. External Power Supply Plug

CAUTION

Do not use the external power supply when the UUT +5 voltage supply exceeds 6.2 volts. Damage may result from excessive current flow from the UUT to the tester.

The type of plug used creates a momentary short circuit across the power supply when it is inserted in the tester back panel socket. Therefore, it is imperative that the plug is plugged into the socket before the power supply is connected to the power outlet.

SYNC/TRIGGER INTERFACE

The SYNC/Trigger Interface is located on the rear panel of the tester. The interface consists of two metal posts where an oscilloscope probe and ground can be clipped. (Refer to Figure 2-2 for location.)

When the tester is executing a Memory or I/O test, the SYNC/Trigger Interface outputs a pulse when the UUT generates a DMA acknowledge signal in response to the tester forcing a DMA request to the UUT. If the tester is not executing a test, the tester outputs a pulse synchronized to the rising edge of the data valid state on the UUT bus for all UUT read/write cycles.

The SYNC/Trigger Interface can also output a pulse when the tester detects a predefined event or condition on the UUT. For more information refer to Break-Point, Frame-Point, or External Trigger in Section 4. The pulse can be used to trigger an oscilloscope or similar equipment.

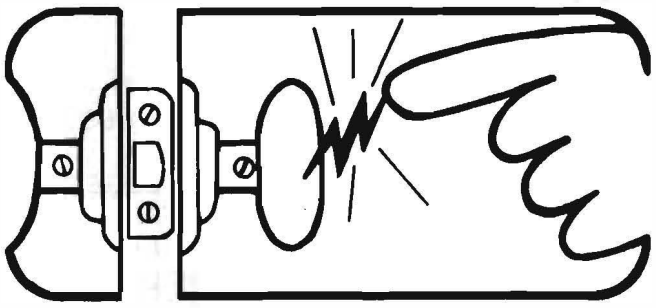
CAUTION

Be sure that you clip the oscilloscope and ground leads to the correct posts, as labeled on the tester. An incorrect connection prevents generation of the SYNC/Trigger pulse.

static awareness

A Message From

John Fluke Mfg. Co., Inc.

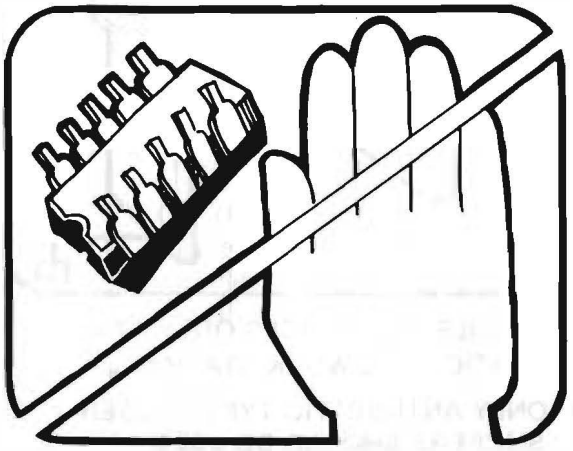


Some semiconductors and custom IC's can be damaged by electrostatic discharge during handling. This notice explains how you can minimize the chances of destroying such devices by:

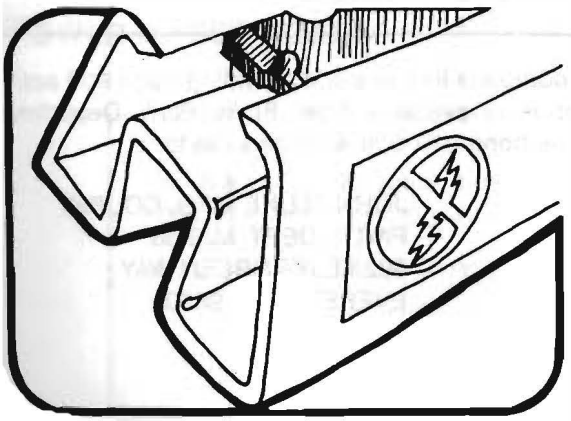
1. Knowing that there is a problem.
2. Learning the guidelines for handling them.
3. Using the procedures, and packaging and bench techniques that are recommended.

The Static Sensitive (S.S.) devices are identified in the Fluke technical manual parts list with the symbol "⊗"

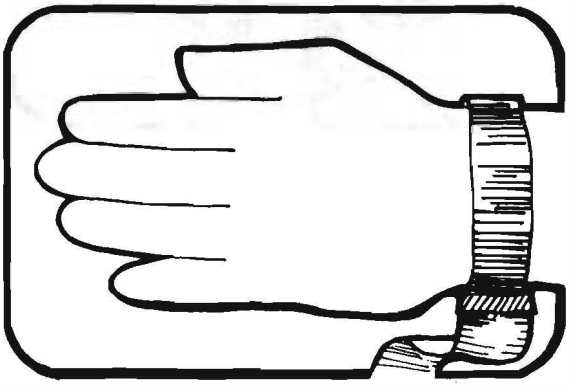
The following practices should be followed to minimize damage to S.S. devices.



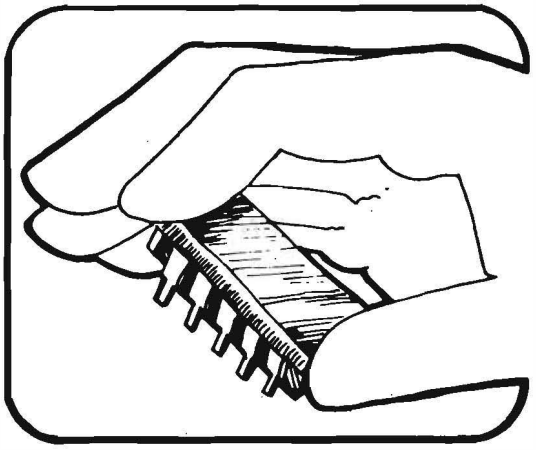
1. MINIMIZE HANDLING



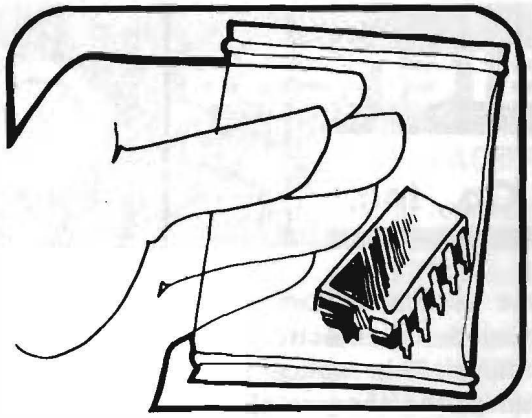
2. KEEP PARTS IN ORIGINAL CONTAINERS UNTIL READY FOR USE.



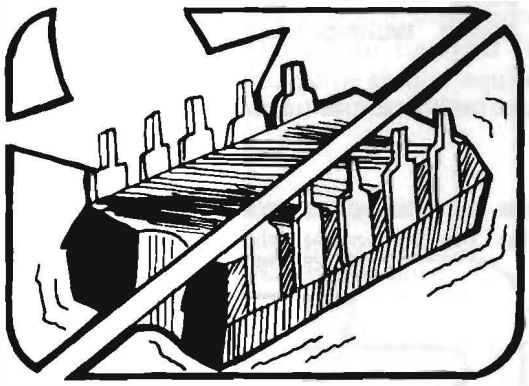
3. DISCHARGE PERSONAL STATIC BEFORE HANDLING DEVICES. USE A HIGH RESISTANCE GROUNDING WRIST STRAP.



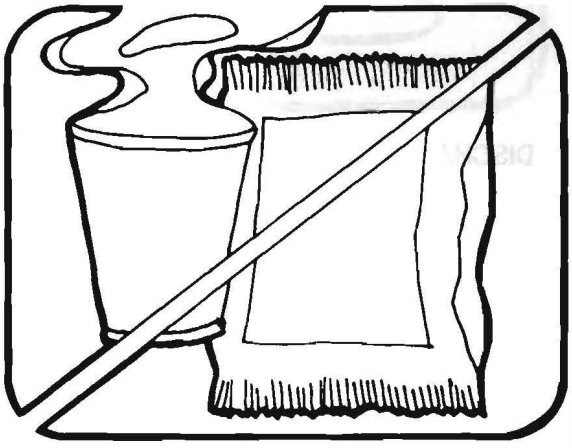
4. HANDLE S.S. DEVICES BY THE BODY



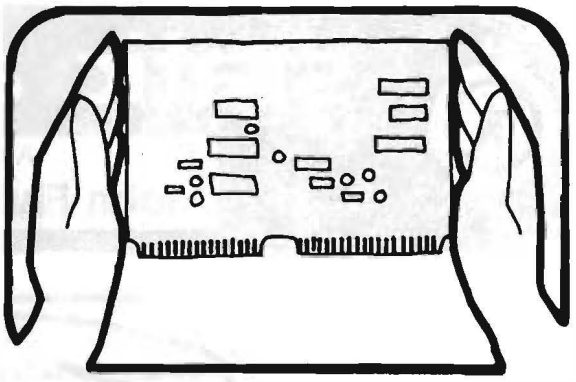
5. USE STATIC SHIELDING CONTAINERS FOR HANDLING AND TRANSPORT



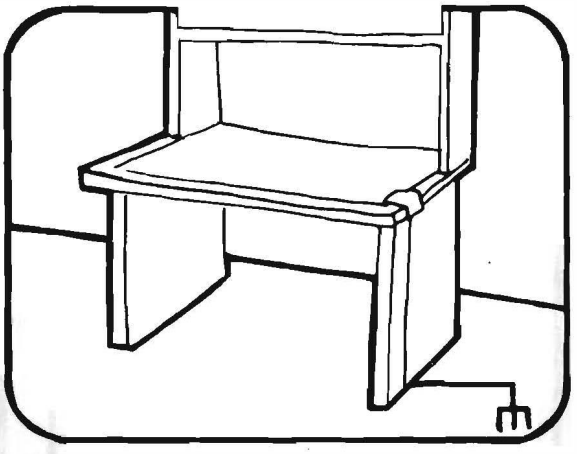
6. DO NOT SLIDE S.S. DEVICES OVER ANY SURFACE



7. AVOID PLASTIC, VINYL AND STYROFOAM® IN WORK AREA



8. WHEN REMOVING PLUG-IN ASSEMBLIES, HANDLE ONLY BY NON-CONDUCTIVE EDGES AND NEVER TOUCH OPEN EDGE CONNECTOR EXCEPT AT STATIC-FREE WORK STATION. PLACING SHORTING STRIPS ON EDGE CONNECTOR HELPS TO PROTECT INSTALLED SS DEVICES.



9. HANDLE S.S. DEVICES ONLY AT A STATIC-FREE WORK STATION

10. ONLY ANTI-STATIC TYPE SOLDER-SUCKERS SHOULD BE USED.

11. ONLY GROUNDED TIP SOLDERING IRONS SHOULD BE USED.

A complete line of static shielding bags and accessories is available from Fluke Parts Department, Telephone 800-526-4731 or write to:

JOHN FLUKE MFG. CO., INC.
PARTS DEPT. M/S 86
9028 EVERGREEN WAY
EVERETT, WA 98204

® Dow Chemical

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Rev. 1 MAR 86

Section 3
Operation

INTRODUCTION

Section 3 explains how to perform tests from the keypad. The organization of this section follows the order in which tests are likely to be performed.

Your tester may not operate properly unless:

- The model of your tester matches the type of microprocessor tested.
- The DMA control line(s) of the UUT microprocessor are free to be driven both high and low (not tied together or tied directly to ground or +5 volts).

NOTE

If the DMA Control line(s) are tied directly to ground, +5 volts, or bussed together, it is necessary to isolate those line(s) by carefully removing them from their socket or desoldering if needed. After all testing is completed, carefully restore the control line(s) to their original state.

- The UUT has an operational +5 volt supply.
- The power supply of the UUT handles the 150 mA current drawn by the tester. (This limitation can be overcome by using the optional external power supply with the tester.)

POWER UP SEQUENCE

Use the following procedure to operate the tester. A detailed procedure for each test is provided under the specific test heading in the remainder of Section 3.

1. With a voltmeter, make sure that the power to the UUT microprocessor does not exceed 6.2V dc. Supply voltage above 6.2V dc may damage the tester.
2. Turn off power to the UUT. Connect the microprocessor clip to the microprocessor on the UUT. (See Figure 3-1.)

CAUTION

Be sure to align pin 1 of the microprocessor clip marked by a white circle to pin 1 of the microprocessor of the UUT.

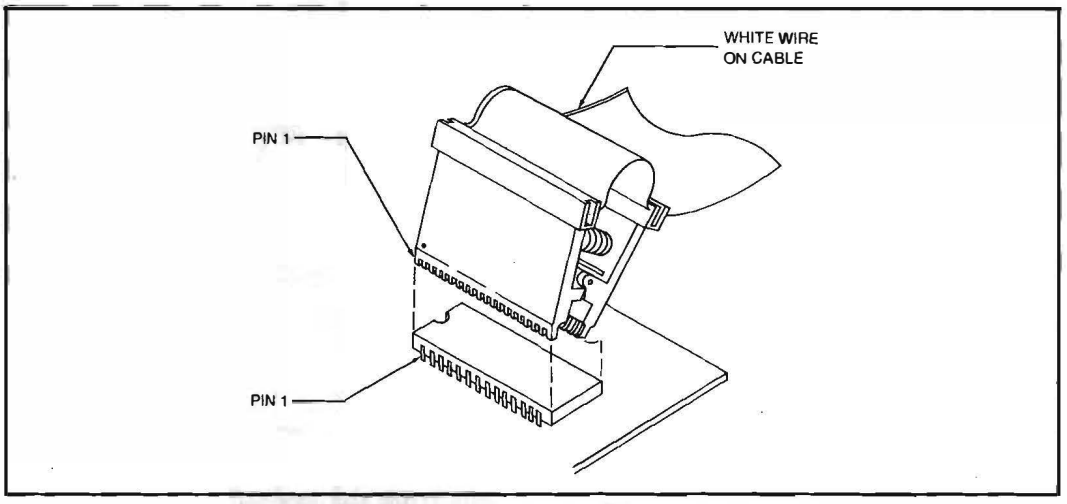


Figure 3-1. Correct Alignment for Microprocessor Clip

3. Turn the power to the UUT back on. The following message flashes on the display:

```
FLUKE-90
Self-Test...
```

A series of Self-Tests, transparent to the user, are run.

If the self-test routine is completed successfully, the following prompt is displayed and output through the Remote Interface:

```
>
MM VERS 2.10
```

The prompt > without "MM VERS 2.10" is displayed whenever the tester is not running a test and is ready to accept a command from the keyboard.

If a failure is detected, the tester halts, and the following message is displayed and output through the Remote Interface:

```
ERROR nnn x---x
x-----------x
```

The message "Error nnn" corresponds to an error code, whose description can be found in Table 3-1. Information represented by "x---x" is a brief description of the error.

4. Select a test category by pressing the BUS TEST, MEM TEST, I/O TEST, or the PROBE key.

Table 3-1. Error Codes

ERROR NUMBER	DESCRIPTION
1	Tester RAM bad
2	Tester LCA bad
3	UUT clock failure
4	UUT DMA request line not drivable
5	UUT DMA acknowledge line not operating
6	UUT wait line not drivable
7	UUT reset line stuck active
8	Tester ROM bad
9	Tester LCD not operating
10	Tester RS-232-C Interface not operating

5. Scroll through the test menu by pressing the same test key repeatedly until the name of the desired test or Probe function is displayed.

6. Press the ENTER key to select a specific test or Probe function.

   - If additional data is not required, the test or Probe function is executed.
   - If additional data is required, a prompt appears on the display. Use the numeric keys (0 to F) to enter data and/or addresses.

   After you have entered the data, press the ENTER key to execute one test cycle.

7. If a fault is detected, an error message is displayed and the current test or Probe function is halted. The error message overwrites whatever is on the display and remains on the display until an input from the user is received.

   - If the ENTER key is pressed, the error message is replaced with the appropriate "test-in-progress" message, and the test or Probe function resumes after the point where the fault was detected.
   - If the LOOP key is pressed, a "test-in-progress" message is displayed, an activity indicator flashes □, and looping begins on the step at which the fault was detected. The error message reappears immediately.
   - Press the CLEAR or RESET key to terminate a test in progress. Remember that pressing the RESET key also resets the UUT.

8. If no fault is detected, the message "TEST COMPLETED" message is displayed.

   - If the ENTER key is pressed, the test restarts.
   - If the LOOP key is pressed, the test continuously runs and a "test-in-progress" message is displayed and the activity indicator flashes until the CLEAR or RESET key is pressed.

9. Press any other Test key or the PROBE key to select another test category.

WARNING

THE TESTER IS NOT GROUND ISOLATED. ENSURE THAT THE MAXIMUM VOLTAGE FROM THE UUT TO EARTH GROUND DOES NOT EXCEED 30V. TO DETERMINE IF THE UUT GROUND IS FLOATING, TAKE A VOLTMETER AND MEASURE THE VOLTAGE BETWEEN A UUT SIGNAL AND A KNOWN EARTH GROUND.

BASIC TESTS

For the tester to work properly, the microprocessor on the UUT must maintain a minimum functional level. The tester monitors the operation of the microprocessor on the UUT by automatically running six Basic Tests at the beginning of every DMA access that the tester executes.

When a Basic Test detects a fault, the appropriate error message is displayed, and any user-selected test is aborted. The error message remains on the display until you enter another command. The six Basic Tests are:

- Power Supply Test
- Clock Test
- DMA Request Line Test
- UUT DMA Acknowledge Line Test
- UUT Wait Line Test
- Reset Line Drivability Test

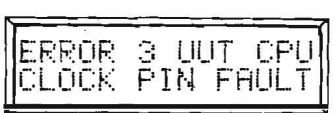
These tests are described in the following paragraphs.

Power Supply Test

A portion of the tester always derives its power from the UUT. If the UUT power supply is inoperable the tester display remains blank and the tester is not operational.

Clock Test

A malfunctioning clock on the the UUT microprocessor can cause the failure of any test execution, and constitutes a fatal error. The clock test senses the rising and falling edges of the clock signal. If both edges of the clock signal are not present, the tester detects a faulty clock, all operations are halted, and the following message is written on the display:



This message stays on the display until you enter another command.

DMA Request Line Test

The tester must be able to drive the DMA request line(s). The tester ensures that these lines are drivable by performing a DMA request line test every time a DMA access is attempted. If the line is not drivable, the tester halts all operations and displays the following message:

```
ERROR 4  UUT CPU
BUS REQUEST FAIL
```

This message remains on the display until you press another key.

UUT DMA Acknowledge Line Test

The UUT microprocessor must generate a DMA acknowledge signal in response to the tester forcing a DMA request. If the DMA acknowledge line does not respond, the following message is displayed:

```
ERROR 5  NO UUT
BUS ACKNOWLEDGE
```

This message remains on the display until you press another key.

UUT Wait Line Test

The tester must drive the UUT wait line. If the UUT wait line is stuck in either a high or low state, the following message is displayed:

```
ERROR 6 UUT CPU
WAIT PIN FAULT
```

This message remains on the display until you press another key.

Reset Line Drivability Test

The tester drives the UUT reset line during and after some tests. If the reset line is stuck, in either a high or low state, the following message is displayed:

```
ERROR 7 UUT CPU
RESET PIN FAULT
```

This message stays on the display until you press another key.

TROUBLESHOOTING FLOWCHART

To assist you in developing a troubleshooting procedure using the tester, a flowchart (Figure 3-2) has been provided. The flowchart begins with connecting the microprocessor dip-clip to the UUT and leading you through a step-by-step troubleshooting procedure.

As you proceed through the flowchart, the hexagonal blocks suggest the type of test to execute, the diamond blocks ask a question for you to make some type of decision, the plain rectangular blocks suggest some type of action, and the bolded rectangular blocks suggest possible repair or replacement of UUT components.

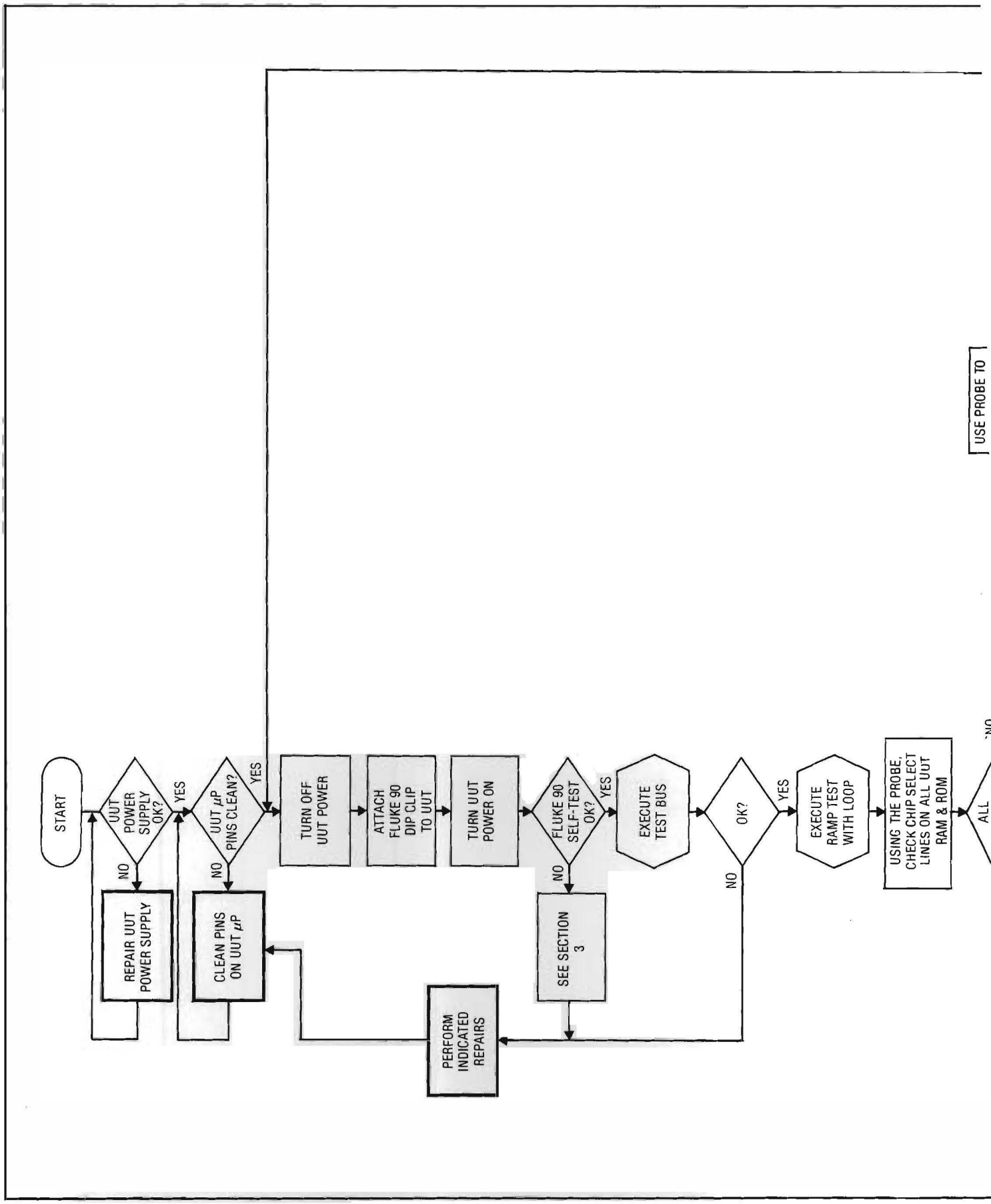
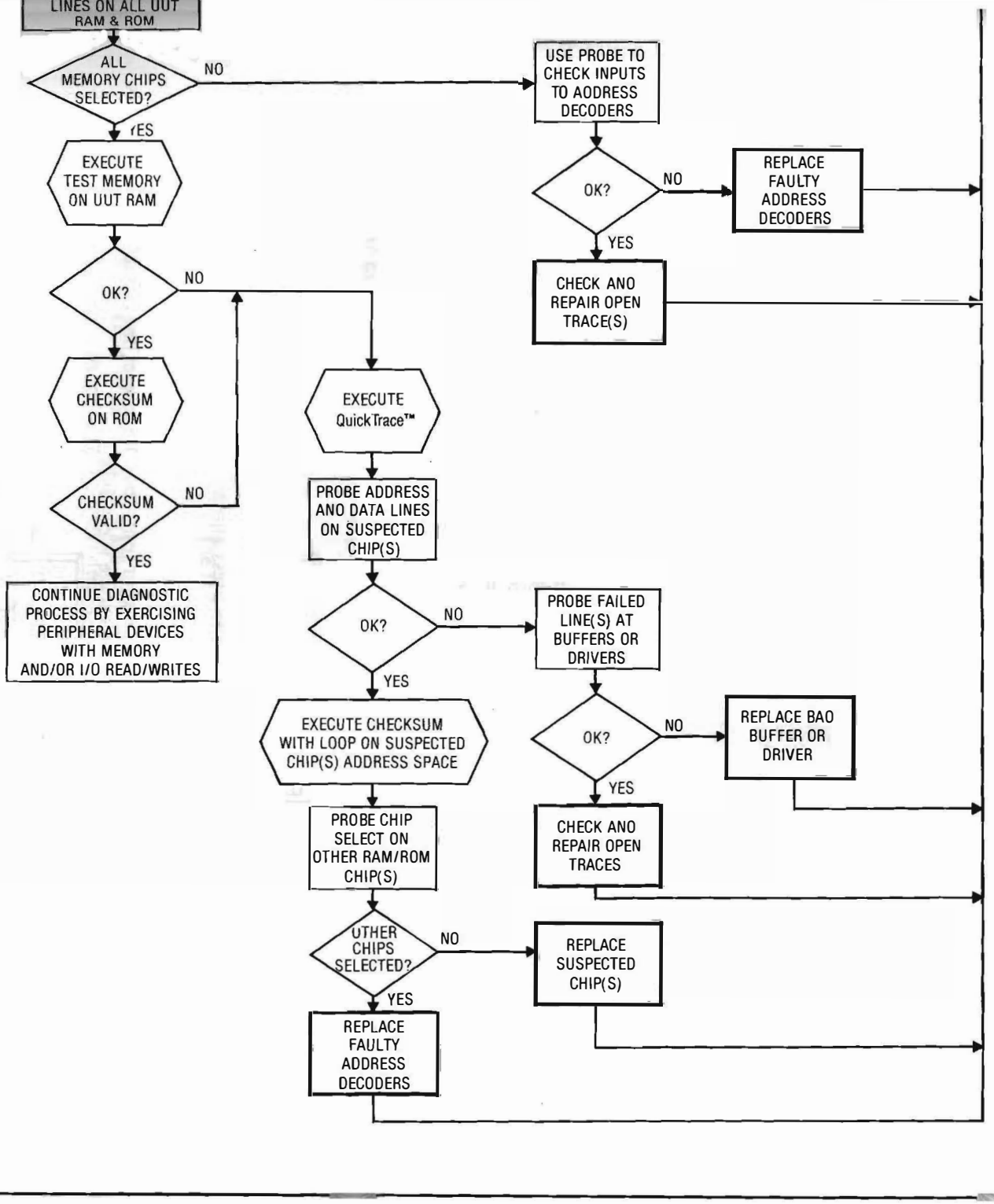


Figure 3-2. Troubleshooting Flowchart


LINES ON ALL OUT RAM & ROM
ALL MEMORY CHIPS SELECTED?
NO
USE PROBE TO CHECK INPUTS TO AODRESS DECODERS
YES
EXECUTE TEST MEMORY ON UUT RAM
OK?
NO
REPLACE FAULTY ADDRESS DECODERS
YES
CHECK ANO REPAIR OPEN TRACE(S)
OK?
NO
YES
EXECUTE CHECKSUM ON ROM
EXECUTE QuickTrace™
CHECKSUM VALID?
NO
YES
PROBE ADDRESS ANO DATA LINES ON SUSPECTED CHIP(S)
CONTINUE DIAGNOSTIC PROCESS BY EXERCISING PERIPHERAL DEVICES WITH MEMORY AND/OR I/O READ/WRITES
OK?
NO
PROBE FAILED LINE(S) AT BUFFERS OR DRIVERS
YES
EXECUTE CHECKSUM WITH LOOP ON SUSPECTED CHIP(S) ADDRESS SPACE
OK?
NO
REPLACE BAO BUFFER OR DRIVER
YES
CHECK ANO REPAIR OPEN TRACES
PROBE CHIP SELECT ON OTHER RAM/ROM CHIP(S)
OTHER CHIPS SELECTED?
NO
REPLACE SUSPECTED CHIP(S)
YES
REPLACE FAULTY ADDRESS DECODERS

BUS TESTS

Introduction

Bus Tests isolate defects in the UUT data, address, and control lines inside the microprocessor kernel. Before testing, make sure that the clip is properly connected to the UUT microprocessor and the tester's self-test routines have been successfully completed. The prompt ⟩ should be on the display.

NOTE

Bus Tests disable the normal operation of the UUT.

Three types of Bus Tests can be executed:

- Test Bus
- Ramp Test
- Shift Test

Test Bus

TYPICAL USES

The primary use of Test Bus is to check for shorts and incorrect connections between UUT components. The test also checks the functionality of the microprocessor kernel.

HOW TEST BUS IS PERFORMED

Test Bus determines the integrity and drivability of address, data, and selected control lines directly attached to the microprocessor inside any latches, buffers, drivers and/or decoders. The Fluke 90 forces the bus lines, one at a time, to specific states. It then senses the state of all the bus lines, detecting whether the line has achieved the desired state and whether other address, data, or control lines are shorted to the signal line being forced.

TROUBLESHOOTING HINTS

- The UUT is held in a DMA state during the test, stopping the operation of the UUT.
- Test Bus does not detect address, data, or control lines that are open or not connected.
- Bus lines outside of any drivers, buffers, latches or decoders are not checked. (See Ramp Test or any of the Probe functions for more information.)
- Control lines checked by QuickTrace are the only control lines tested. (See decal on the bottom of the instrument for the control lines tested.)

BUS TESTS

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Bus Tests isolate defects in the UUT data, address, and control lines inside the microprocessor kernel. Before testing, make sure that the clip is properly connected to the UUT microprocessor and the tester's self-test routines have been successfully completed. The prompt > should be on the display.

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- Control lines checked by QuickTrace are the only control lines tested. (See decal on the bottom of the instrument for the control lines tested.)

EXECUTING TEST BUS

1. Press the BUS TEST key to enter the Bus Test menu. The display shows the name of the last Bus Test performed. Press the BUS TEST key repeatedly to scroll through the possible Bus Tests, until "TEST BUS" appears on the display.

2. Press the ENTER key to start the Test Bus test. While the test is running, "TEST BUS" is displayed and the activity indicator flashes on the screen.

   If the test does not detect a fault, the following message is displayed:

   ```
   TEST BUS
   TEST COMPLETED
   ```

   If an error is detected, the following message is displayed:

   ```
   TEST BUS FAIL @
   signalname level
   ```

   In the second line of the message, "signalname" is the name of the faulty signal and "level" is either "HI" or "LO".

   If the LOOP key is pressed, the tester continues to test the failed line until the CLEAR key is pressed or the failure is removed. Press the ENTER key to display any additional failure messages.

3. After one test cycle has been run, you can run the test again by pressing the ENTER key. Press LOOP to cause the test to be run in a continuous loop.

4. To stop a test cycle at any time, press the CLEAR or RESET key.

Ramp Test

TYPICAL USES

The Ramp Test determines faulty address decoder and buffer outputs connected to the UUT bus. The test also determines if the UUT address and/or data lines are shorted or connected improperly.

A memory write cycle is performed to all UUT memory space addresses during the Ramp Test, which should enable all UUT address decoders. The output of the address decoders can be monitored using the Probe. Any lack of activity during the test, may be an indication of a faulty component.

HOW RAMP TEST IS PERFORMED

The Ramp Test outputs an incremented pattern on all address and data lines. (See Figure 3-3.) For each new pattern, the tester performs a memory write cycle that enables any address decoders, buffers, or drivers. Activity can be verified for each signal line, with the use of the Probe or an oscilloscope. Lack of activity may be an indication of a faulty component.

Address or data line shorts, or improper connections outside the UUT kernel can be detected by observing frequency activity of the selected line with respect to its neighboring lines. For example, if address line 13 (A13) is of interest, the next lower line (A12) should toggle (low/high/low) at twice the frequency of A13 and the next higher line (A14) should toggle at half the frequency of A13.

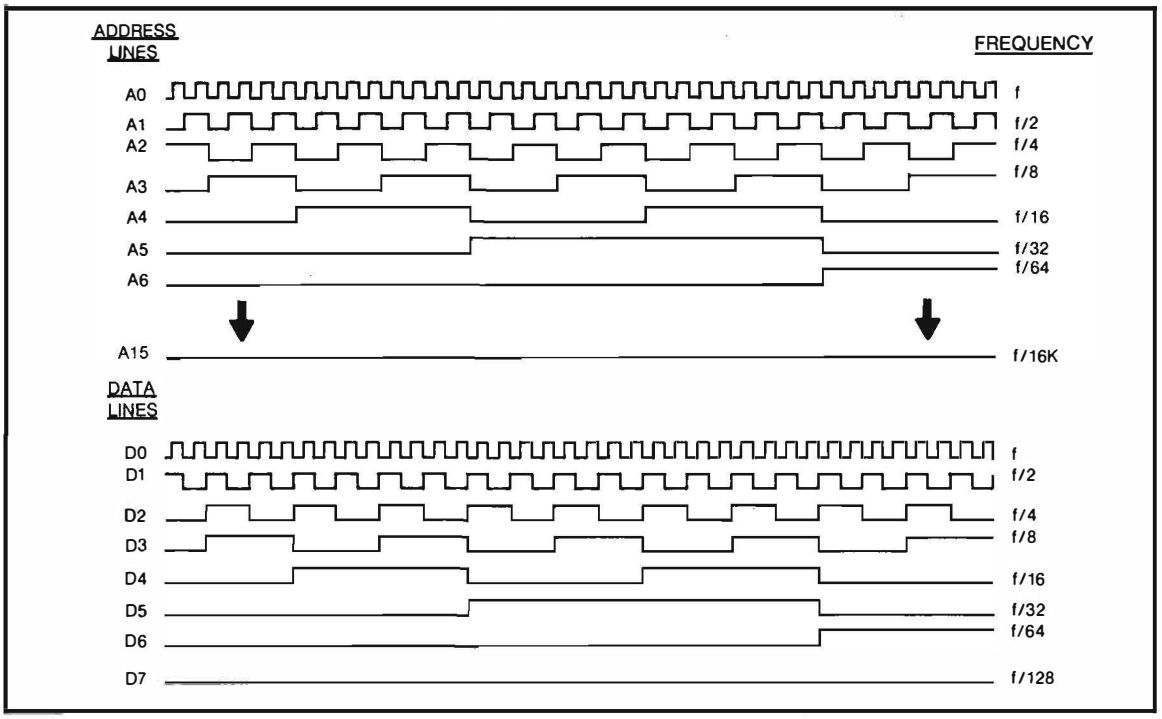


Figure 3-3. Ramp Test Waveform

TROUBLESHOOTING HINTS

- During the test, the UUT is held in a DMA state and UUT operation is not possible.
- Care must be taken with UUT microprocessors that have positive true Bus Request signals (BUSREQ: inactive low and active high). If the line is driven directly by a TTL or CMOS gate, the pin must be disconnected from the board, or a 10 kilohm pull-up resistor placed in series with the gate and the microprocessor pin.
- Only bus drivability is tested, no checks are performed on the RAM or ROM of the UUT. (See Test Memory and Checksum for more information.)
- The UUT control lines are not exercised. (See Probe Control or QuickTrace for more information.)
- Monitoring the frequency of the low order address and data lines may require the use of an oscilloscope to observe Ramp Test wave forms. At high frequencies the Probe lights are lit continuously and activity frequency can not be observed.

EXECUTING RAMP TEST

1. Press the BUS TEST key to enter the Bus Test menu. The name of the last Bus Test performed is displayed. Press the BUS TEST key repeatedly to scroll through the possible bus tests, until "RAMP TEST" appears on the display.

2. Press the ENTER key to start the Ramp test. While the test is running, "RAMP TEST" is displayed and the activity indicator flashes on the screen.

3. At the end of one test cycle, the following message is displayed:

```
RAMP TEST
TEST COMPLETED
```

4. After one test cycle has been completed, you can execute the test again by pressing the ENTER key. Press LOOP to cause the test to be run in a continuous loop.

   While the Ramp Test is running in loop mode, you can use the Probe and/or an oscilloscope to detect shorts or opens in UUT address and data lines.

   Starting at the lowest order address or data line, check each signal line for a decreasing frequency square wave. For example, when probing the data lines, D1 shows a signal of ½ the frequency or twice the period of D0. If the same frequency is found on two lines, these lines are shorted together.

5. To stop a test cycle at any time, press the CLEAR or RESET key.

Shift Test

TYPICAL USES

The Shift Test detects shorted or stuck UUT address and data lines. With the use of the Probe or an oscilloscope, activity on these lines can be observed. Lack of activity may be an indication to the location of a fault.

HOW SHIFT TEST IS PERFORMED

The Shift Test, or walking-bit test, rotates a logic 1 through all address and data lines. (See Figure 3-4.) The Shift Test is different from the Ramp Test in that the Shift Test forces only one address (or data) line high at a time.

Like the Ramp Test, a memory write is performed for each new bit pattern. During the execution of the Shift test only one bit is enabled and address decoders may not be exercised. Shorts between address and/or data lines may be easier to locate with the Shift test rather than with the Ramp test, because only one address or data line is active at a time.

TROUBLESHOOTING HINTS

- During the test, the UUT is held in a DMA state and normal UUT operation is not possible.
- The UUT address decoders are not fully exercised due to the lack of signal line activity. (See Ramp Test for more information.)
- The UUT control lines are not tested. (See Probe Control or QuickTrace for more information.)

EXECUTING SHIFT TEST

1. Press the BUS TEST key to enter the Bus Test menu. The display shows the name of the last Bus Test performed. Press the BUS TEST key repeatedly to scroll through the possible Bus Tests, until "SHIFT TEST" appears on the display.

2. Press the ENTER key to start the Shift Test. While the test is running, the activity indicator flashes on the screen.

3. At the end of one test cycle, the following message is displayed:

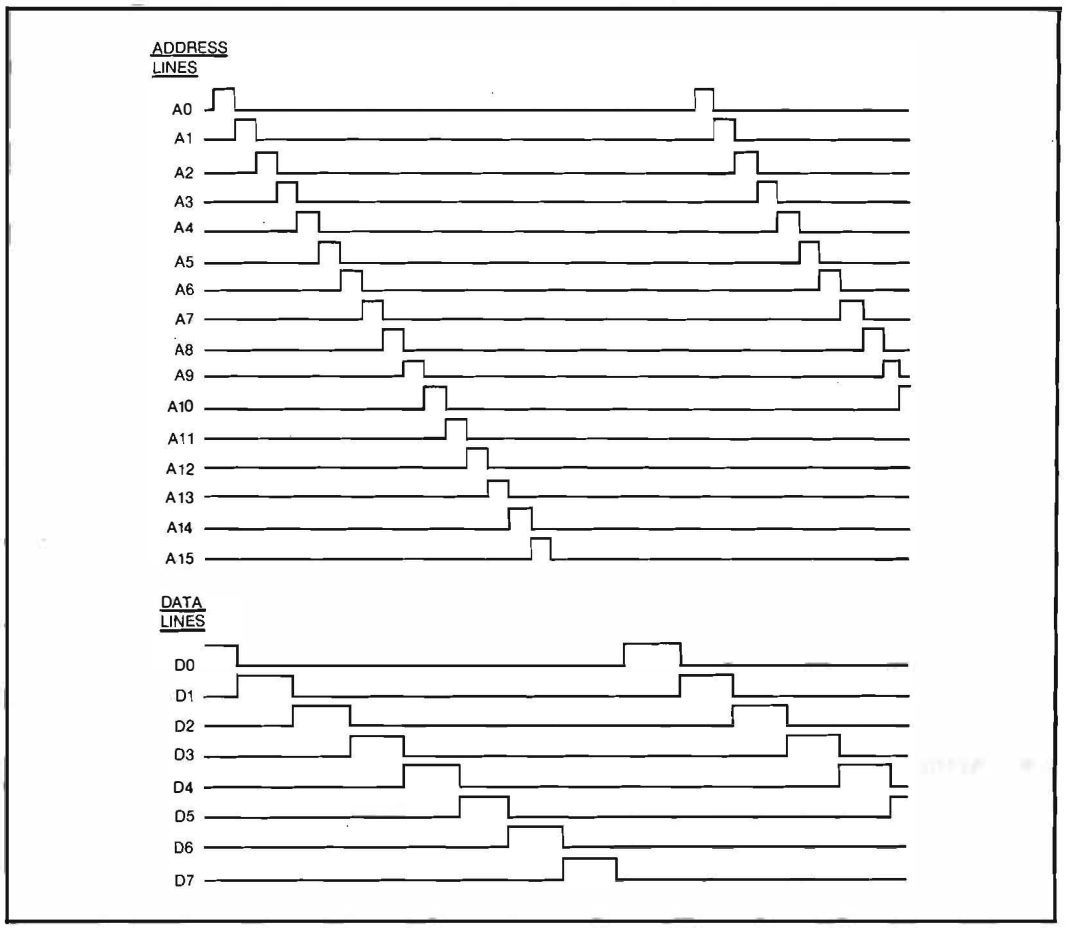


Figure 3-4. Shift Test Waveform

4. After one test cycle has been run, you can run the test again by pressing the ENTER key. Press LOOP to cause the test to be run in a continuous loop so that an oscilloscope or the Probe may be used to detect shorts or opens in the UUT address/data bus.

5. To stop a test cycle at any time, press the CLEAR or RESET key.

MEMORY TESTS

NOTE

The UUT bus and kernel must be operational. Run the Bus Tests first before Memory Tests.

Introduction

Memory Tests detect faults in memory and memory-related elements of the UUT. The tester forces memory read and write cycles on the UUT bus.

Six Memory Tests can be executed:

- Test Memory
- Checksum Test
- Memory Examine
- Memory Verify
- Memory Write
- Memory Soak

These tests (except for Memory Soak) do not disturb the normal operation of the UUT. However, the Test Memory and Checksum Test tests require a large amount of bus time and may slow normal UUT operations.

Some UUTs have timer circuits that reset the UUT microprocessor if it is inactive for a long period of time. It may be necessary to defeat this timer when using the Test Memory, Checksum Test, and Memory Soak tests.

Before testing, make sure that the clip is properly connected to the UUT microprocessor and the tester's self-test routines have been successfully completed. The prompt ⟩ should be on the display.

Test Memory

TYPICAL USES

Test Memory non-destructively exercises the UUT RAM to verify its functionality and determine if any faults occur.

NOTE

It is recommended that you first execute Test Bus, Ramp Test, or QuickTrace to make sure that the UUT bus is operational before executing Test Memory.

Test Memory can be operated in a LOOP mode, so that memory failures due to thermal stress can be induced by heating/cooling suspected chip(s) while Test Memory is executing.

HOW TEST MEMORY IS PERFORMED

For each selected memory location, the contents are read, two patterns (55 Hex and AA Hex) are written, verified, and the original contents restored.

Test Memory does not halt the normal operation of the UUT, but operates in a cycle-stealing mode. Some slowing of UUT operation may be observed during test execution. The total time for the read/write operations is controlled so that dynamic RAM remains refreshed.

TROUBLESHOOTING HINTS

- Due to shorts or faulty memory decoders, simultaneous inadvertent reads and writes to multiple memory addresses are possible. In normal operation each memory cell is tested individually. (See Memory Checksum for more information.)

- Static RAM sometimes exhibit a failure mode where it fails to retain its contents after a period of time. Since the write/ read cycle is very short, the cycle may not be detected with Test Memory. (See Memory Soak for more information.)

EXECUTING TEST MEMORY

1. Press the MEM TEST key to enter the Memory Test menu. The display shows the name of the last Memory Test performed. Press the MEM TEST key repeatedly to scroll through the possible Memory Tests until "TEST MEMORY" appears on the display.

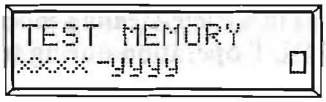
2. Press the ENTER key. The display shows the following prompt:

   The last starting address is represented by "xxxx". Use the numeric entry keys to enter the start address in hexadecimal.

3. Press the ENTER key. The display shows the following prompt:

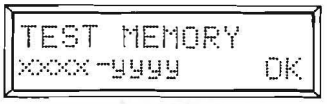
   The last ending address entered is represented by "yyyy". Enter the ending address in hexadecimal and press the ENTER key to start the Memory Test.

4. During test execution the activity indicator flashes and the following message is displayed:



   The starting address and ending address is represented by "xxxx-yyyy".

5. At the completion of the test, the following message appears on the display if no fault is detected:



If the test detects a fault the following message appears on the display:

The address where the fault is detected is represented by "zzzz", "aa" is the pattern written (AA Hex or 55 Hex) to the location, and "bb" is the pattern read.

6. If you press the ENTER key after the first test cycle, the test is repeated. If you press the LOOP key, the test is performed continuously. If the test fails, the error message is displayed and the test is suspended. Press the ENTER key to continue the test, or the LOOP key to loop the test on the address where the test failure occurred. If the failure is intermittent, the test continues from the address where the failure occurred until another failure is encountered.

Checksum Test

TYPICAL USES

Checksum Test verifies the operation of ROM in the UUT.

NOTE

It is recommended that you first execute Test Bus, Ramp Test, or Quick-Trace to make sure that the UUT bus is operational before executing Checksum Test.

Checksum Test can also be used to check for suspected faulty address decoders for both RAM and ROM. All memory locations within the selected address range are accessed. The selected address range can be used to test a single memory chip and the Probe can be used to check the chip select lines on other memory chip(s). If any other chip select activity is present, it may indicate a faulty address decoder.

HOW CHECKSUM TEST IS PERFORMED

Checksum Test tests the ROM in the UUT by reading the data from the specified range and accumulating the 16-bit sum of this data. This checksum is equivalent to what is generated by most EPROM programming equipment.

Checksum Test operates in a cycle-stealing mode and does not interrupt UUT operation. Some slowing of UUT operation during test execution may be observed.

TROUBLESHOOTING HINTS

- During the execution of Checksum Test, the tester reads each memory cell individually. Shorts or faulty memory decoders may cause erroneous reads.
- Some UUTs use memory-mapped I/O that changes state when examined. Check the UUT design information first for warnings directed at this situation before executing this test on non-RAM/ROM addresses.

EXECUTING CHECKSUM TEST

1. Press the MEM TEST key to enter the Memory Test menu. The display shows the name of the last Memory Test performed. Press the MEM TEST key repeatedly to scroll through the possible Memory Tests until "CHECKSUM TEST" appears on the display.

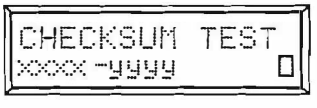
2. Press the ENTER key. The display shows the following prompt:

   The last start address entered is represented by "xxxx". Use the numeric entry keys to enter the start address in hexadecimal.

3. Press the ENTER key. The display shows the following prompt:

   The last end address entered is represented by "yyyy". Enter the end address in hexadecimal, and press ENTER to start the Checksum Test.

4. During the test the activity indicator flashes and the following message is displayed:



5. At the completion of the test, the following message appears on the display:

   The starting address and the ending address is represented by "xxxx-yyyy" and "zzzz" is the checksum computed.

6. If you press the ENTER key after the first test cycle, the test is repeated once. If you press the LOOP key after the first test cycle, the test is executed continuously until the CLEAR or the RESET key is pressed.

Memory Examine

TYPICAL USES

Memory Examine is used to examine the contents of any memory-mapped location in the address space of the UUT.

NOTE

It is recommended that you first execute Test Bus, Ramp Test, or QuickTrace to make sure that the UUT bus is operational before executing Memory Examine.

When Memory Examine is used in the LOOP mode. the Probe can be used to check that only the proper memory address is accessed.

HOW MEMORY EXAMINE IS PERFORMED

An address value is entered through the user keypad. The tester reads the contents of that address and displays its contents.

TROUBLESHOOTING HINTS

- During the execution of Memory Examine, erroneous reads are possible because of faulty RAM/ROM, shorts, or faulty memory decoders. It is recommended that you first execute Test Bus, Ramp Test, or QuickTrace to determine if the memory decoders and drivers are functioning properly.

- Some UUT microprocessors use memory-mapped I/O that changes state when examined. Check the UUT design information first for this situation before performing this test on non-RAM/ROM addresses.

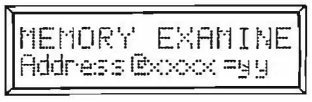
EXECUTING MEMORY EXAMINE

1. Press the MEM TEST key to enter the Memory Test menu. The display shows the name of the last Memory Test performed. Press the MEM TEST key repeatedly to scroll through the Memory Test menu, until "MEMORY EXAMINE" appears on the display.

2. Press the ENTER key. The display shows the following prompt:

   The last address entered is represented by "xxxx". Use the numeric entry keys to enter the address in hexadecimal.

3. Press the ENTER key. The following message appears on the display:



   The address and the data at that address is represented by "xxxx" and "yy" respectively.

4. If at this point, you press the LOOP key to execute this test in the loop mode, a read continues to be performed on the same address, the following message is displayed, and the activity indicator flashes until the CLEAR key or the RESET key is pressed:

5. To increment the address by 1 and examine the contents of the new address, press the ENTER key. Hold the ENTER key down to cause continuous incrementing of the address and display of the new address and data.

Memory Verify

TYPICAL USES

Memory Verify is used to write to a memory address and then verify that the data written is still contained at that location.

NOTE

It is recommended that you first execute Test Bus, Ramp Test, or QuickTrace to make sure that the UUT is operational before executing Memory Verify.

When Memory Verify is used in the LOOP mode, the Probe can be used to check that only the proper memory address is accessed.

HOW MEMORY VERIFY IS PERFORMED

After you enter the address and data, the tester writes the specified data into a memory address, reads the same address, and compares the data read to what was written. The read and write operations are performed on the same DMA cycle to prevent the UUT from overwriting the data.

Memory Verify is the preferred test to change the contents of RAM, because this test performs a read-after-write operation.

TROUBLESHOOTING HINTS

- During the execution of Memory Verify erroneous reads are possible because of faulty RAM, shorts, or faulty memory decoders. It is recommended that you first execute Test Bus, Ramp Test, or QuickTrace to determine if the memory decoders and drivers are functioning properly.

- Some UUT microprocessors use memory-mapped I/O that changes state when examined. Check the UUT design information first for this situation before performing this test on non-RAM addresses.

EXECUTING MEMORY VERIFY

1. Press the MEM TEST key to enter the Memory Test menu. The display shows the name of the last Memory Test performed. Press the MEM TEST key repeatedly to scroll through the possible Memory Tests, until "MEMORY VERIFY" appears on the display.

2. Press the ENTER key. The display shows the following prompt:

   The last address entered is represented by "xxxx". Use the numeric entry keys to enter the starting address in hexadecimal.

3. Press the ENTER key. The displays shows the following prompt:

   The last data entered is represented by "yy".

4. Enter new data and press the ENTER key to execute the test. When the test cycle is complete the following message appears on the display:

   The address and the data read is represented by "xxxx" and "yy" respectively. If the read and write do not match, the following message appears on the display:

   The data written and the data read is represented by "aa" and "bb" respectively.

5. If you press the ENTER key after the first test cycle, the address is incremented by 1, and the display shows a prompt for new data. Enter new data or simply press the ENTER key to repeat the test with previously entered data.

6. If after the first test cycle, you press the LOOP key, the test is repeated in a continuous loop at the same address until you press the CLEAR or RESET key. If a fault occurs during the LOOP mode the activity indicator stops flashing and the message that appears on the display is the same as in Step 4.

Memory Write

TYPICAL USES

Memory Write is used to write data to a specific UUT memory location.

NOTE

It is recommended that you first execute Test Bus, Ramp Test, or QuickTrace to make sure that the UUT bus is operational before executing Memory Write.

When Memory Write is used in the LOOP mode, the Probe can be used to check that only the proper memory address is accessed.

HOW MEMORY WRITE IS PERFORMED

After you enter address and data values, the tester writes the entered data into a UUT memory address. The data written to the address space is not read back as with Memory Verify.

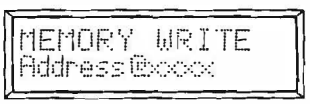
TROUBLESHOOTING HINTS

- During the execution of Memory Write, erroneous writes are possible because of faulty RAM, shorts, or faulty memory decoders. It is recommended that you first execute Test Bus, Ramp Test, or QuickTrace to determine if the address decoders and drivers are functioning properly.

EXECUTING MEMORY WRITE

1. Press the MEM TEST key to enter the Memory Test menu. The display shows the name of the last Memory Test performed. Press the MEM TEST key repeatedly to scroll through the possible Memory Tests, until "MEMORY WRITE" appears on the display.

2. Press the ENTER key. The display shows the following prompt:



   The last address entered is represented by "xxxx". Use the address/data entry keys to enter the address in hexadecimal.

3. Press the ENTER key. The display shows the following prompt:

   The last data written is represented by "yy".

4. Enter new data and press ENTER to execute the test. When the test cycle is complete the following message appears on the display:

   The address and data written is represented by "xxxx" and "yy" respectively.

5. If you press the ENTER key after the first test cycle, the address is incremented by 1, and the display prompts you for new data. Enter new data or simply press the ENTER key to repeat the test with previously entered data.

6. If you press the LOOP key after the first test cycle, the test is repeated in a continuous loop (using the same data) at the same address until you press the CLEAR key or RESET key.

Memory Soak

TYPICAL USES

Memory Soak is used to determine that data written to static RAM of the UUT is retained for a specified period of time.

NOTE

It is recommended that you first execute Test Bus, Ramp Test, or QuickTrace to make sure that the UUT bus is operational before executing Memory Soak.

Memory Soak (with a soak time of 0) may also be used to fill a specified range of memory.

HOW MEMORY SOAK IS PERFORMED

After you enter the address range, data, and soak time, the Memory Soak test writes the data to the address range. The tester counts down the specified time period, and at the end of the soak time compares the contents against the data written.

The UUT is held in a DMA state during this test to prevent the RAM contents from being overwritten.

TROUBLESHOOTING HINTS

- During the execution of the Memory Soak test, the UUT is held in a DMA state, and all UUT operation is suspended. This test may not be suitable for dynamic memory.

- Care must be taken with UUT microprocessors that have positive true Bus Request signals (BUSREQ: inactive low and active high). If the line is driven directly by a TTL or CMOS gate, the pin must be disconnected from the board, or a 10 kilohm pull-up resistor placed in series with the gate and the microprocessor pin.

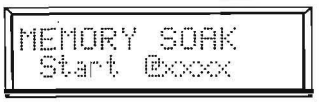
- Some UUT microprocessors use memory-mapped I/O that changes state when examined. Check the UUT design information first for this situation before performing this test on non-RAM addresses.

- During the execution of Memory Soak, the operation of the UUT is temporarily suspended. However, inactivity detector circuits (software activated) may force the UUT through its power up restart sequence. It is suggested that any inactivity detector circuit be disabled before executing Memory Soak.

EXECUTING MEMORY SOAK

1. Press the MEM TEST key to enter the Memory Test menu. The display shows the name of the last Memory Test performed. Press the MEM TEST key repeatedly to scroll through the possible Memory Tests until "MEMORY SOAK" appears on the display.

2. Press the ENTER key. The display shows the following prompt:



   The last start address entered is represented by "xxxx". Use the numeric entry keys to enter the start address in hexadecimal.

3. Press the ENTER key. The display shows the following prompt:

   The last end address entered is represented by "yyyy". Use the numeric entry keys to enter the end address in hexadecimal.

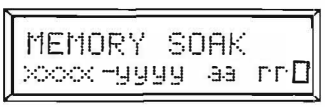
4. Press the ENTER key. The display shows the following prompt:

   The previous data entered is represented by "aa". Enter a data pattern.

5. Press the ENTER key. The display shows the following prompt:

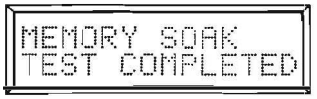
   The last soak time entered is represented by "tt". Enter a time between 0 to 99 minutes.

6. Press the ENTER key to start the test. While the test is in progress, the activity indicator flashes and the following message is displayed:



   The starting and ending address is represented by "xxxx-yyyy". The user-specified pattern, and the soak time remaining is represented by "aa" and "rr" respectively.

7. After the soak time has elapsed, the following message is displayed if no failure has been detected:



or the following message is displayed if a failure has been detected:

The address of the first detected error is represented by "zzzz", and the pattern written and read at that address is represented by "aa" and "bb" respectively. Press the ENTER key to display any additional error messages.

8. If you press the ENTER key after the first test cycle, the test repeats once. If you press the LOOP key after the first test cycle, test is repeated in a continuous loop until you press the CLEAR or RESET key.

I/O TESTS

Introduction

I/O tests exercise I/O addresses and are similar to the Memory Tests except that the I/O Tests use I/O access bus cycles rather than memory cycles.

NOTE

If the microprocessor of the UUT does not support a separate I/O address space, the display shows the message, "NOT SUPPORTED" when one of the three I/O tests is selected.

Three I/O tests (and the RS-232-C port configuration function) are available on the I/O TEST key. The I/O tests are:

- I/O Examine
- I/O Verify
- I/O Write

I/O Examine

TYPICAL USES

I/O Examine is used to examine the contents of a specified UUT I/O address.

NOTE

It is recommended that you first execute Test Bus before executing I/O Examine as a normal troubleshooting procedure.

When I/O Examine is used in the LOOP Mode, the Probe can be used to check that only the proper I/O address is accessed.

HOW I/O EXAMINE IS PERFORMED

An I/O address value is entered through the user keypad. The tester accesses that address in the UUT I/O address space and displays its contents.

TROUBLESHOOTING HINTS

- Reading I/O addresses can cause state changes in the I/O circuits. Check the UUT design information first for warnings directed at this situation before performing this test.

EXECUTING I/O EXAMINE

1. Press the I/O TEST key to enter the I/O Test menu. The display shows the name of the last I/O Test performed. Press the I/O TEST key repeatedly to scroll through the possible I/O Tests until "I/O EXAMINE" appears on the display.

2. Press the ENTER key. The display shows the following message:

   The last address entered is represented by "xx". Use the numeric keys to enter the address in hexadecimal.

3. Press the ENTER key. The following message is displayed:

   The address and data at that address is represented by "xx" and "yy" respectively.

4. Press the ENTER key to increment the address by 1 and examine the contents of the new address. Hold the ENTER key down to cause continuous incrementing of the address and display of the new address and data.

5. Press the LOOP key to execute this test in the loop mode. A read is performed on the same address, and the following message is displayed. The activity indicator flashes until you press the CLEAR or RESET key.

I/O Verify

TYPICAL USES

I/O Verify is used to write to an I/O address and then verify that the written data is still contained at that I/O address.

NOTE

It is recommended that first you execute Test Bus before executing I/O Verify as a normal troubleshooting procedure.

HOW I/O VERIFY IS PERFORMED

After you enter the I/O address and data value, the tester writes the data to the specified I/O address, then reads the same address and compares the data read to what was written. The read and write operations are performed on the same DMA cycle to prevent the UUT from overwriting the data.

TROUBLESHOOTING HINTS

- I/O Verify performs a read-after-write operation and may return unexpected data or cause state changes in the I/O circuits. Check the UUT design information first for warnings directed at this situation before performing this test.

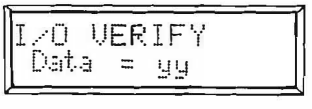
EXECUTING I/O VERIFY

1. Press the I/O TEST key to enter the I/O Test menu. The display shows the name of the last I/O Test performed. Press the I/O TEST key repeatedly to scroll through the possible I/O Tests until "I/O VERIFY" appears on the display.

2. Press the ENTER key. The display shows the following prompt:

   where "xx" represents the last address entered. Use the numeric keys to enter the start address in hexadecimal.

3. Press the ENTER key. The tester displays the following message:



   The last data entered is represented by "yy".

4. Enter new data and press the ENTER key to execute the test. When the test cycle is complete the following message appears on the display.

The address and the data read at that address is represented by "xx" and "yy" respectively.

If the read and write do not match the following message appears on the display:

The data written and read at the verified I/O address is represented by "aa" and "bb" respectively.

5. If you press the ENTER key after the first test cycle, the address is incremented by 1, and the display issues a prompt for new data. Enter new data or simply press the ENTER key to repeat the test with previously entered data.

6. If you press the LOOP key after the first test cycle, the test is repeated in a continuous loop at the same address until you press the CLEAR or RESET key. If a fault occurs during the LOOP mode the activity indicator stops flashing and the message in the display is the same as Step 4.

I/O Write

TYPICAL USES

The I/O Write test is used to write entered data to a specified UUT I/O address.

NOTE

It is recommended that you execute Test Bus first before executing I/O Write as a normal troubleshooting procedure.

When I/O Write is used in the LOOP mode, the Probe can be used to check that only the proper I/O address is accessed.

HOW I/O WRITE IS PERFORMED

After you enter the I/O address and data value, the tester writes the data to the I/O port address specified.

TROUBLESHOOTING HINTS

- Writing to I/O addresses can cause state changes in the I/O circuits. Check UUT design information first for this situation before this test.

EXECUTING I/O WRITE

1. Press the I/O TEST key to enter the I/O Test menu. The display shows the last I/O Test performed. Press the I/O TEST key repeatedly to scroll through the possible I/O Tests, until "I/O WRITE" appears on the display.

2. Press the ENTER key. The display shows the following prompt:

The last address entered is represented by "xx". Use the numeric keys to enter the start address in hexadecimal.

3. Press the ENTER key. The display shows the following prompt:

The last data entered is represented by "aa".

4. Enter data and press the ENTER key to execute the test. When the test cycle is complete the following message appears on the display:

The address and data written at that address is represented by "xx" and "bb" respectively.

5. If you press the ENTER key after the first test cycle the address is incremented by 1, and the display shows a prompt for new data. Enter new data or simply press the ENTER key to repeat the test with the previously entered data.

6. If you press the LOOP key after the first test cycle, the test is repeated in a continuous loop (using the same data) at the same address until you press the CLEAR or RESET key.

RS-232-C Port Configuration

The RS-232-C port configuration is not an I/O test. It allows the tester and an external terminal or computer to communicate with the correct baud rate and bits per character. You can set the baud rate (300, 600, 1200, 2400, 4800, or 9600) and bits per character (7 or 8) for the RS-232-C Remote Communications Interface from the keyboard as well as by a Remote Interface Command. See Section 4 and Appendix A for the Configuration command.

Use the following procedure to set the baud rate and bits per character:

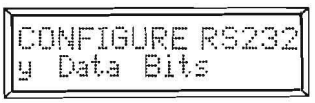
1. Press the I/O TEST key to enter the I/O Test menu. The display shows the name of the last I/O Test performed. Press the I/O TEST key repeatedly to scroll through the possible I/O Tests, until "CONFIGURE RS232" appears on the display.

2. Press the ENTER key. The display shows the following prompt:

The default (1200) value or the last baud rate entered is represented by "xxxx".

3. Press the LOOP key repeatedly until the desired baud rate appears on the display.

4. Press the ENTER key and the display shows the following prompt:



   either 7 or 8 (the default value) data bits per character is represented by "y".

5. Press the LOOP key until the desired data bit length is displayed. Then press the ENTER key to complete the configuration sequence.

These settings are returned to the default values of 1200 baud and 8 bits per character when power is removed. The non-changeable parameters of the RS-232-C Interface are no parity and one stop bit.

USING THE PROBE

Introduction

The Probe included with the tester can be used to isolate faults in UUT data, address, and control lines not directly connected to the microprocessor. The Probe can function as either a Logic Probe synchronized to the data valid state of the UUT bus, or possess the following specific functions:

- QuickTrace
- Probe Address Lines
- Probe Data Lines
- Probe Control Lines

CAUTION

When you exit a Probe Function, the UUT is reset.

Probe Description

The Probe is a hand-held device shown in Figure 2-4 that plugs into a connector on the rear panel of the tester and detects signal states on the UUT. The Probe has a push button, a red light, and a green light. The push button on the Probe has the same function as the ENTER key on the tester keypad. It allows you to increment to the next signal line without touching the tester.

If the signal being probed is in the high state (or the Probe is not touching a valid digital signal), the red light on the Probe is lit. If the signal is in the low state, the green light is lit. If the signal is toggling between a high and low state, both red and green lights flash rapidly at a rate that depends on the frequency of the signal (the higher the frequency, the higher the flash rate).

Whenever the tester is not executing a test, the Probe is synchronized to the data valid state of the UUT bus. When the tester is executing a test (bus, memory, or I/O), the Probe is synchronized with the data valid state of the UUT bus on read or write cycles forced by the tester.

QuickTrace

TYPICAL USES

QuickTrace can be used to rapidly isolate and follow suspected faulty address, data, or control line(s) in the UUT. By starting at a known good location (for example, the microprocessor), the signal line can be probed to isolate the fault.

NOTE

Not all control lines may be identified by QuickTrace, Refer to the decal on the bottom of the instrument for the control lines tested.

HOW QUICKTRACE IS PERFORMED

The QuickTrace function causes the tester to continually search for the signal line being probed. During the execution of QuickTrace, a memory write cycle is forced to allow identification of address and data lines of outside buffers or drivers. When the probed line is identified, the lights on the Probe toggle from red to green, and the signal probed is identified.

TROUBLESHOOTING HINTS

- Care must be taken with UUT microprocessors that have positive true Bus Request signals (BUSREQ: inactive low and active high). If the line is driven directly by a TTL or CMOS gate, the pin must be disconnected from the board, or a 10 kilohm pull-up resistor placed in series with the gate and the microprocessor pin.

- During execution of QuickTrace, the UUT microprocessor is held in a DMA state and UUT operation is halted.

- The decal on the bottom of the tester identifies the control lines that can be tested by your instrument.

- Lines shorted to Vcc or ground can not be identified using QuickTrace. (See Test Bus or Ramp Test for information on detecting shorted signal lines.)

- During the execution of QuickTrace, the operation of the UUT is temporarily suspended. However, inactivity detector circuits (software activated) may force the UUT through its power up restart sequence. It is suggested that any activity detector circuit be disabled before executing QuickTrace.

EXECUTING QUICKTRACE

1. Press the PROBE key to enter the Probe menu. The display shows the name of the last Probe function performed. Press the PROBE key repeatedly to scroll through the possible PROBE menu selections until "QuickTrace" appears on the display.

2. Press the ENTER key. The activity indicator flashes, QuickTrace is displayed, and the red Probe light is on while the test is running before any signal line is probed.

3. Make contact between the Probe and a bus signal. Upon recognition of the signal, the Probe lights change from red to green, the activity indicator continues to flash, and the following message appears on the display:

The signal name probed (BUS, MEMORY, CONTROL) is represented by "nnnn". If you are sure that the proper signal has been probed and the red light remains on, the signal is either shorted or stuck high or low.

Each time you probe a testable signal line, the tester identifies the name of the signal.

When a node with two or more signals connected to it is probed, both lights on the probe are lit and all signal names are displayed.

To clear the display of the last probed signal mains, press the button on the Probe or the ENTER key.

4. Press the CLEAR or RESET key to stop the test.

Probe Address

TYPICAL USES

Probe Address is used with the Probe to test UUT microprocessor address lines. The Probe Address function sequentially prompts the probing of all address lines. During the execution of Probe Address, a memory write cycle is forced to allow identification of address lines outside buffers or drivers.

HOW PROBE ADDRESS IS PERFORMED

Once you have selected the Probe Address function, you are prompted to identify which address line to probe. When the requested address line is probed, the lights on the probe toggle from red to green. Select the next address line by pressing ENTER on the keyboard, or by pressing the button on the Probe.

TROUBLESHOOTING HINTS

- Care must be taken with UUT microprocessors that have positive true Bus Request signals (BUSREQ: inactive low and active high). If the line is driven by a TTL or CMOS gate, the pin must be disconnected from the board, or a 10 kilohm pull-up resistor placed in series with the gate and the microprocessor pin.

- During execution of Probe Address, the UUT microprocessor is held in a DMA state and UUT operation is halted.

- Lines shorted to Vcc or ground can not be identified using Probe Address. See Test Bus or Ramp Test for information on detecting shorted signal lines.

- During the execution of Probe Address the operation of the UUT is temporarily suspended. However, inactivity detector circuits (software activated) may force the UUT through its power up restart sequence. It is suggested that any inactivity detector circuit be disabled before executing Probe Address.

EXECUTING PROBE ADDRESS

1. Press the PROBE key to enter the Probe menu. The display shows name of the last Probe function performed. Press the PROBE key repeatedly to scroll through the possible PROBE menu selections until "PROBE ADDRESS" appears on the display.

2. Press the ENTER key. While the test is running but before a signal is probed, the activity indicator flashes and the following message appears on the display:

   The (decimal) number of the address line to be probed is represented by "aa". To select the desired line, press the ENTER key or the button located on the Probe to increment, or press the LOOP key to decrement.

3. Make contact between the Probe and the address line. When the correct signal is probed, the green Probe light goes on and the red light goes out. The activity indicator stops flashing and the following message appears on the display:

   If you are sure that the proper signal has been probed and the red Probe light remains on, the signal is either shorted or stuck high or low.

4. To select the next line to be probed, press the button on the Probe or press the ENTER key. To scroll back to a previous signal, press the LOOP key until the prompt for the desired address signal number is displayed.

5. To stop the test at any time, press the CLEAR or RESET key.

Probe Data

TYPICAL USES

Probe Data is used in conjunction with the Probe to test UUT microprocessor data lines. The Probe Data function sequentially prompts the probing of all data lines. During the execution of Probe Data, a memory write cycle is forced to allow identification of data lines outside buffers or drivers.

HOW PROBE DATA IS PERFORMED

Once you have selected the Probe Data function, you are prompted to probe a data line. When the requested data line is probed, the lights on the probe toggle from red to green. Select the next data line by pressing ENTER on the keyboard, or by pressing the button on the probe.

TROUBLESHOOTING HINTS

- Care must be taken with UUT microprocessors that have positive true Bus Request signals (BUSREQ: inactive low and active high). If the line is driven directly by a TTL or CMOS gate, the pin must be disconnected from the board, or a 10 kilohm pull-up resistor placed in series with the gate and the microprocessor pin.

- During execution of Probe Data, the UUT microprocessor is held in a DMA state and UUT operation is halted.

- Lines shorted to Vcc or ground can not be identified using Probe Data. See Test Bus or Ramp Test for information on detecting shorted signal lines.

- During the execution of Probe Data, the operation of the UUT is temporarily suspended. However, inactivity detector circuits (software activated) may force the UUT through its power up restart sequence. It is suggested that any inactivity detector circuit be disabled before executing Probe Data.

EXECUTING PROBE DATA

1. Press the PROBE key to enter the Probe menu. The display shows the name of the last Probe function performed. Press the PROBE key repeatedly to scroll through the possible PROBE menu selections until "PROBE DATA" appears on the display.

2. Press the ENTER key. While the test is running but before a signal is probed, the activity indicator flashes and the following message appears on the display:

   The (decimal) number of the last data line to be probed is represented by "d". To select the desired line, press the ENTER key or the Probe button to increment, or press the LOOP key to decrement to the next data line.

3. Make contact between the Probe and the data line. When the correct signal is probed, the green light turns on and the red light goes out. The following message appears on the display:

   If you are sure that the proper signal has been probed and the red Probe light remains on, the signal is either shorted or stuck high or low.

4. To select the next signal to be probed, press the button on the probe or press ENTER. To scroll back to a previous signal, press LOOP until the prompt for the desired data signal number is displayed.

5. To stop the test at any time, press the CLEAR or RESET key.

Probe Control

TYPICAL USES

Probe Control is used with the Probe to test UUT microprocessor control lines. The Probe Control function sequentially prompts the probing of the control lines associated with the UUT microprocessor.

HOW PROBE CONTROL IS PERFORMED

Once you have selected the Probe Control function, you are prompted to identify which control line to probe. When the requested control line is probed, the lights on the probe toggle from red to green. Select the next control line by pressing ENTER on the keyboard, or by pressing the button on the probe.

TROUBLESHOOTING HINTS

- Care must be taken with UUT microprocessors with positive true Bus Request signals (BUSREQ: inactive low and active high). If the line is driven directly by a TTL or CMOS gate, the pin must be disconnected from the board, or a 10 kilohm pull-up resistor placed in series with the gate and the microprocessor pin.
- During execution of Probe Control, the UUT microprocessor is held in a DMA state and UUT operation is halted.
- Lines shorted to Vcc or ground can not be identified using Probe Control.
- The control lines identified on the bottom decal of the instrument are the only control lines tested.
- During the execution of Probe Control, the operation of the UUT is temporarily suspended. However, inactivity detector circuits (software activated) may force the UUT through its power up restart sequence. It is suggested that any inactivity detector circuit be disabled before executing Probe Control.

EXECUTING PROBE CONTROL

1. Press the PROBE key to enter the Probe menu. The display shows name of the last Probe test performed. Press the PROBE key repeatedly to scroll through the possible PROBE menu selections until "PROBE CONTROL" appears on the display.

2. Press the ENTER key. While the test is running but before a signal is probed, the activity indicator flashes and the following message appears on the display:

   The name of the last control line probed is represented by "cccc". To select the desired line, press the ENTER key or the button on the Probe to increment, or press the LOOP key to decrement to the next control line number.

3. Make contact between the Probe and the control line. When the correct signal is probed, the green light goes on and the red light goes out. The following message appears on the display:

   If you are sure that the proper signal has been probed and the red Probe light remains on, the signal is either shorted, or stuck high.

4. To select the next signal to be probed, press the button on the Probe or press the ENTER key. To scroll back to a previous signal, press the LOOP key until the prompt for the desired control signal number is displayed.

5. To stop the test at any time, press the CLEAR or RESET key.

Section 4
Remote Operations

INTRODUCTION

The tester can be operated as a stand-alone unit (in local mode) or in conjunction with a host or terminal (in remote mode). In the local mode, all commands are issued from the keypad of the tester; in the remote mode, all commands are transmitted over an RS-232-C communications interface.

Local/Remote and Remote Commands

All tests and functions executed in the local mode, are also executable in the remote mode. Additional functions can be executed only over the RS-232-C interface. Section 4 covers the commands, tests, and functions that are executed remotely. (Local operation is described in Section 3.)

Remote Testing

Remote testing can be performed interactively or by using a computer program. In interactive testing, you enter commands at a terminal keyboard, the tester responds, and results are printed to the screen. Remote testing by program requires that the tester commands be included in a computer program which, when executed, controls the testing process.

REMOTE COMMUNICATIONS INTERFACE

Remote operation communication is conducted through an RS-232-C interface connector located on the rear panel of the tester. See Table 4-1 and Figure 4-1 for the pin-out and pin location of the connector. The connector is a 6-line, RJ-12 modular connector. Only one point-to-point connection to a single computer or terminal interface is possible. The interface does not support modem control lines.

The active lines of the interface consist of Transmitted Data, Received Data, and Ground. The baud rate for this interface is selectable between 300, 600, 1200, 2400, 4800, and 9600. With a loss of power the tester resets to the 1200 baud default value. The interface can be configured for either 7 or 8 bits per character; the default value is 8 bits. The interface is configured for one stop bit per character and no parity. These settings cannot be changed.

XON (13H, ^Q) and XOFF (11H, ^S) characters control character flow. An XOFF character from the terminal or host computer stops character flow from the tester and an XON character from the terminal or host computer resumes character flow.

Table 4-1. RS-232-C Connector Pin-Out

PIN NUMBER	DATA LINES
P1	No Connection
P2	Ground
P3	Receive Data (input to tester)
P4	Transmit Data (output from tester)
P5	Ground
P6	No Connection

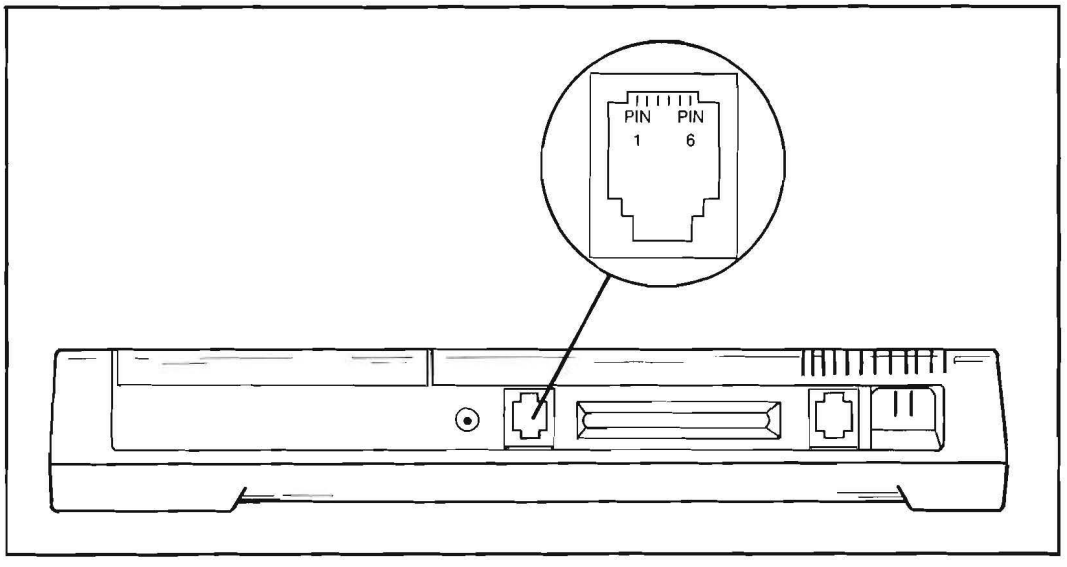


Figure 4-1. RS-232-C Interface Connector

CABLING TESTER TO A TERMINAL OR HOST

The RS-232-C cable shipped with the tester is terminated by an RJ-12 compatible plug at both ends. One end plugs into the RJ-12 connector on the tester; the other end plugs into an adapter that connects to the serial port on the terminal or host computer.

The tester is cabled to a terminal or host as shown in the system illustration on the inside cover of this manual.

CAUTION

Do not plug the tester into a telephone wall jack. Damage to the tester circuitry may result.

SYNC/TRIGGER INTERFACE

The SYNC/Trigger interface is located on the rear panel of the tester. The interface consists of two metal posts to which a probe and ground of an oscilloscope can be clipped. The External Trigger commands using the SYNC/Trigger interface can be issued remotely only.

CAUTION

Be sure that you clip oscilloscope and ground leads to the correct posts, as labeled on the tester. A misconnection results in a nongeneration of the SYNC/Trigger pulse.

If the tester is being operated in the remote mode, the SYNC/Trigger interface can be enabled or disabled. If the SYNC/Trigger interface is enabled, a trigger pulse is output only when the tester detects a selected event that is defined by a Break-Point, Frame-Point, or External Trigger command. (See "Break-Point, Frame-Point, and External Trigger Commands" later in Section 4.) If the SYNC/Trigger interface is disabled (the default condition), a pulse is output when the UUT generates a DMA Acknowledge signal in response to the tester forcing a DMA Request. Whenever the tester is not executing a test, the External Trigger on a memory read is the default state and generates a negative going pulse on the rising edge of data valid after you hit a ⟨CTRL⟩ X. You have to enable the trigger output with the ⟨CTRL⟩ X command before the tester outputs trigger pulses.

An "ESC" character disables all External Trigger, Frame-Point, and Break-Point setups and returns the system to a default state of External Trigger on a memory read. Use ⟨CTRL⟩ X to enable External Trigger, Frame-Point, and Break-Point.

OVERVIEW OF REMOTE OPERATION

Control Commands

The Control commands provide the control functions indicated in Table 4-2 when you are operating the tester remotely.

The first character received by the tester (sent by the host or terminal) on the remote interface causes the display to read "REMOTE" and locks the keypad. Press the CLEAR the key to unlock the keypad and return the tester to local operation.

A Control command is executed on the terminal by holding down the ⟨CTRL⟩ key on the keyboard, while simultaneously pressing the appropriate letter key.

NOTE

The symbol ^ means ⟨CTRL⟩.

Table 4-2. Control Commands

COMMAND	HEX VALUE	FUNCTION	KEYPAD EQUIVALENT
^X	10	Step or Continue	ENTER
^Q	11	Resume Transmission (XON)	None
^S	13	Pause Transmission (XOFF)	None
^B or ⟨ESC⟩	02	Terminate Command	CLEAR

Test Or Command Execution Sequence

In the remote mode, a command or test is executed as follows:

1. The tester prompts for input by sending the message ENTER⟩ (or ENTER⟩⟩ if a Break-Point is enabled). Right angle brackets "⟩⟩" indicate that the UUT has been halted in a Break-Point mode only. If you send a Break-Point or Frame-Point by a ⟨CR⟩, the current status is displayed.

2. A test is started when the tester receives a valid command line over the remote interface.

   A valid command line consists of a syntactically correct string of commands, constants, variables, and options that is terminated by a carriage return (⟨CR⟩). If an illegal command is received, the tester responds with the message ???? ⟨CR⟩ followed by a prompt.

3. Remote commands can be executed in a single test cycle or loop mode. To start the loop mode, append the optional "/L" flag to a test command line.

   In the loop mode, a command is executed continually until the tester receives the control command, "^B," (control B - O2 Hex) or ⟨ESC⟩.

4. If the Test fails, the tester displays the string "FAILED" prompt followed by additional information about the failure and a ⟨CR⟩.

5. Advance to the next step by sending a ^X (control X).

6. Terminate a command or test by sending a ^B or ⟨ESC⟩ to the tester. (You can also terminate the test by pressing the CLEAR or RESET key.)

7. ^X must be sent after a command line in order to enable the setup of External Trigger, Break-Point, or Frame-Point. Each following Frame-Point or Break-Point is "stepped" by successive ^X commands (single step on current setup).

SYNTAX NOTATION CONVENTIONS

The following notation conventions are used to represent the syntax of the commands described in this section. All numbers are hexadecimal unless otherwise indicated.

XX — Unenclosed, upper case letters represent a command that must be entered precisely as given.

Example: BT

means enter "BT" for a Bus Test.

⟨XX⟩ — Angle brackets enclosing upper case letters represent a non-printing ASCII character.

Example: ⟨CR⟩

means CARRIAGE RETURN (or RETURN) character.

x_x Underscoring between elements of a command line represents a mandatory space.

Example: MT_(low-address)_(high-address)[/L]

means that a mandatory space must follow the left parenthesis and precede the low and high address values in this statement.

(xxxx) Parentheses enclose required values.

Example: MT_(low-address)_(high-address)

means you must provide a low and a high address to execute a memory test.

[xxxx] Square brackets enclose optional values.

Example: BT[/L]

means that the /L flag, which will initiate the loop mode, is optional.

x...x Periods between elements represent multiple fields.

Example: MW_(low-address)_(data)_[data]..._[data][/L]

means that multiple data values can be written when a Write Memory test is executed.

REMOTE COMMANDS

The following commands can only be issued over the Remote Interface.

NOTE

Break-Point, Frame-Point, and External Trigger are remote commands that are normally used only by experienced technicians and design or test engineers. These commands are treated separately at the end of Section 4.

NOTE

The (low-address) and (high-address) parameters on the remote command syntax lines can contain up to four-digit hexadecimal numbers.

Memory-Fill Command

The Memory-Fill command writes a single, user-selected, data byte, to an inclusive range of addresses in the UUT. The command line syntax is as follows:

MF_(low-address)_(high-address)_(data)⟨CR⟩

Up-Load Command

The Up-Load command reads data at an inclusive range of addresses in the microprocessor of the UUT and transfers the data read to a terminal or computer. The command line syntax is as follows:

UP_(low address)_(high address)[format]⟨CR⟩

The data transmitted using the Up-Load command may be sent in your choice of two formats: INTEL® HEX or Motorola® HEX. Motorola format is used when the /M appears in the command line. The INTEL format is used when /M does not appear in the command line.

Down-Load Command

The Down-Load command fills memory locations with data through the remote interface. The data is transferred in INTEL HEX (no /M) or Motorola HEX (/M included) format.

The command line syntax is as follows:

DN[format]⟨CR⟩
(data line)⟨CR⟩
[data line]⟨CR⟩
.
.
.
[last data line]⟨CR⟩

Both formats contain internal beginning and ending address information so there is no need to enter address information with this command.

Reset UUT Command

The Reset UUT command resets the UUT microprocessor and associated circuitry. The command does not reset the tester. In response to this command, the tester forces the UUT RESET line active and then releases it. The command line syntax is as follows:

RH[/L]⟨CR⟩

If the optional /L flag is included on the command line, the tester forces a UUT reset over and over again in a continuous loop. There is a 1 second delay between each cycle of this loop.

*INTEL is a registered trade mark of the INTEL Corporation
*Motorola is a registered trade mark of the Motorola Corporation

Transmit Message Commands

The Transmit Message commands are used to display messages on the tester display. The commands can be used to display prompts and other data on the tester display. The command line syntax is as follows:

T1(m)⟨CR⟩
T2(m)⟨CR⟩

The (m)essage prompt represents no more than sixteen characters (including spaces).

The T1 command line fills the upper 16-character line on the LCD, and the T2 command fills the lower 16-character line.

Intercept Keypad Command

The Intercept Keypad command interrupts the normal operation of the tester keypad. The moment any one of the 24 keys are pressed, the labeled action of the key is not interpreted by the tester, but instead sent to the remote computer or terminal.

The command line syntax to enable the Intercept Keypad command is as follows:

EC⟨CR⟩

For example, when the Intercept Keypad command is used, you can enter UUT serial numbers or other identifying information from the tester keypad instead of using the remote computer keyboard.

If you press an address/ data entry key (one of 16 keys in the middle of the keypad) the tester sends the associated ASCII character for the digit. The other six keys send ASCII characters as shown in Table 4-3.

Three different actions may be taken to disable the intercept keypad command. The ENTER key may be pressed from the tester keypad, or ^B or ⟨ESC⟩ may be entered at the remote interface. Once one of the three actions have been taken, the tester sents a "⟨CR⟩⟨LF⟩" character sequence to the remote interface and the tester keypad returns to normal operation.

REMOTE EXECUTION OF LOCAL/REMOTE COMMANDS

Introduction

Local/ Remote commands are commands that can be executed from the tester keypad or sent to the tester from a host computer or terminal through the RS-232-C interface.

If the optional /L flag is included on a command line, that command is executed in a continuous loop until the tester receives a ^B (02 hex) or by pressing the CLEAR or RESET key.

Table 4-4 is a list of local/ remote commands. The list is divided into groups of related commands. Refer to Section 3 for a functional description of a particular test.

Table 4-3. Intercept Keypad Command ASCII Character List

KEY	CHARACTER	HEX VALUE
LOOP	G	47
CLEAR	H	48
BUS TEST	I	49
MEM TEST	J	4A
I/O TEST	K	4B
PROBE	L	4C

Table 4-4. Local/Remote Commands

TEST KEYS	COMMAND
BUS TESTS	
Test Bus	BT[/L] ⟨CR⟩
Ramp Test	RT[/L] ⟨CR⟩
Shift Test	SH[/L] ⟨CR⟩
MEMORY TESTS	
Test Memory	MT_(la)_(ha)[/L] ⟨CR⟩
Checksum Test	CK_(la)_(ha)[/L] ⟨CR⟩
Memory Examine	MX_(la)_(ha)[/L] ⟨CR⟩
Memory Verify	MV_(la)_(d)_[d]...._[d][/L] ⟨CR⟩
Memory Write	MW_(la)_(d)_[d]...._[d][/L] ⟨CR⟩
Memory Soak	MS_(la)_(ha)_(d)_(st)[/L] ⟨CR⟩
Memory Fill	MF_(la)_(ha)_(d) ⟨CR⟩
I/O TESTS	
I/O Examine	IX_(lp)_(hp)[/L] ⟨CR⟩
I/O Verify	IV_(lp)_(d)_[d]...._[d][/L] ⟨CR⟩
I/O Write	IW_(lp)_(d)_[d]...._[d][/L] ⟨CR⟩
RS232 Configure	CP(_b)(_db)
PROBE FUNCTIONS	
QuickTrace	QT
Probe Address Lines	PA
Probe Data Lines	PD
Probe Control Lines	PC

NOTES:

b = baud rate	(300, 600, 1200, 2400, 4800, or 9600)
d = data	(Hexadecimal number 00 to FF)
db = data bits	(7 or 8)
la = low address	(Four-digit, hexadecimal number 0000 to FFFF)
ha = high address	(Four-digit, hexadecimal number 0000 to FFFF)
lp = low port address	(Two-digit, hexadecimal number 00 to FF)
hp = high port address	(Two-digit, hexadecimal number 00 to FF)
st = soak time	(Time in minutes between 0 and 99)

An example using the Memory Soak command using the Remote Interface is as follows:

MS_8000_8FFF_3E_5⟨CR⟩

In the preceding example, the command line translates into a command to perform a Memory Soak test beginning at address 8000 Hex and ending at address 8FFF Hex. The data value written is 3E Hex, and the soak time is 5 minutes.

BREAK-POINT, FRAME-POINT, AND EXTERNAL TRIGGER FUNCTIONS

Introduction

NOTE

The Break-Point, Frame-Point, and External Trigger functions are normally used only by experienced technicians and design or test engineers.

The Break-Point, Frame-Point, and External Trigger functions allow you to take a snapshot look at the UUT bus and associated circuits when a defined event occurs. These commands are mutually exclusive and are available only through the remote interface. See Table 4-5 for a quick reference of these three functions.

- A Break-Point command causes the tester to suspend the programmed operation of the UUT when the event is detected (puts the UUT microprocessor in a HALT or WAIT mode), and displays information about UUT address and data lines.
- A Frame-Point command causes the tester to display the status of UUT address and data lines at a specific event. The programmed operation of the UUT microprocessor is not suspended when the event is detected.
- The External Trigger command causes the tester to generate a SYNC /Trigger pulse at a specific event. The command does not suspend the programmed operation of the UUT microprocessor when that specific event is detected.

Table 4-5. Remote Function Capabilities

FUNCTION	HALTS UUT	CAPTURES ADDRESS AND DATA VALUES	OUTPUTS SYNC/TRIGGER PULSE ON MATCH
Break-Point	Yes	Yes	Yes
Frame-Point	No	Yes	Yes
External Trigger	No	No	Yes

The event that triggers a Break-point, Frame-point or External Trigger command is selected from a list of qualifiers. The qualifiers fall into two categories: the CPU Function qualifiers and General Function qualifiers.

NOTE

When Break-Point, Frame-Point, or External Trigger are enabled, a SYNC/ Trigger pulse is generated only when the selected event is detected.

Command Syntax

The command line syntax for Break-Point, Frame-Point, and External Trigger is summarized in Table 4-6.

CPU Function Qualifiers (Required)

The commands for the CPU Function qualifiers are listed in Table 4-7 These qualifiers control the activation of a Break-Point, Frame-Point, or External Trigger command to the indicated CPU event. One CPU Function qualifier is always required on the command line and only one CPU function may be active at a time. If you select a new CPU function is while another is active, the old function is disabled.

MEMORY READ CPU QUALIFIER

The memory read CPU function qualifier causes the tester to execute the selected function (Break-Point, Frame-Point, or External Trigger) when data is read from memory. If no general qualifiers are specified, all memory read operations cause the selected function to execute.

MEMORY WRITE CPU QUALIFIER

The memory write CPU function qualifier causes the tester to execute the selected function (Break-Point, Frame-Point, or External Trigger) when data is written to memory. If no general qualifiers are specified, all memory write operations cause the selected function to execute.

I/O READ CPU QUALIFIER

The I/O read CPU function qualifier causes the tester to execute the selected function (Break-Point, Frame-Point, or External Trigger) when data is read from an I/O address. If no general qualifiers are specified, all I/O read operations cause the selected function to execute.

I/O WRITE CPU QUALIFIER

The I/O write CPU function qualifier causes the tester to execute the selected function (Break-Point, Frame-Point, or External Trigger) when data is written to an I/O address. If no general qualifiers are specified, all I/O write operations cause the selected function to execute.

OPCODE FETCH CPU QUALIFIER

The opcode fetch CPU function qualifier causes the tester to execute the selected function (Break-Point, Frame-Point, or External Trigger) when the UUT reads an opcode (UUT CPU instruction) from memory. If no general qualifiers are specified, the tester executes the selected function for every instruction execution (single step).

INTERRUPT ACKNOWLEDGE CPU QUALIFIER

The interrupt acknowledge CPU function qualifier causes the tester to execute the selected function (Break-Point, Frame-Point, or External Trigger) when the UUT responds to an interrupt request. If no general qualifiers are specified, the tester executes the selected function for every interrupt generated.

Table 4-6. Break-Point, Frame-Point, and External Trigger Syntax

COMMAND NAME	COMMAND LINE SYNTAX
Break-Point	BP(/cpu)[/gen]...[/gen]⟨CR⟩
Frame-Point	FP(/cpu)[/gen]...[/gen]⟨CR⟩
External Trigger	XT(/cpu)[/gen]...[/gen]⟨CR⟩
Disable BP, FP, XT	DB⟨CR⟩
Break-Point Status	BP*
Frame-Point Status	FP*
External Trigger Status	XT*

NOTES:

/cpu is a required CPU Function qualifier.
/gen is an optional General Function qualifier.
* without CPU or General Function qualifier appended, BP, FP, and XT commands respond with status condition.

Table 4-7. CPU Function Qualifiers

COMMAND	DESCRIPTION
/RE	Enable BP, FP, or XT on Memory Read
/WE	Enable BP, FP, or XT on Memory Write
/IRE	Enable BP, FP, or XT on I/O Read
/IWE	Enable BP, FP, or XT on I/O Write
/OE	Enable BP, FP, or XT on OpCode Fetch
/IE	Enable BP, FP, or XT on Interrupt Acknowledge

General Function Qualifiers (Optional)

The general function qualifiers (summarized in Table 4-8) control the activation of a Break-Point, Frame-Point, or External Trigger and its CPU function qualifier to the indicated condition(s). The general functions qualifiers are optional and may be combined (in any combination).

The following paragraphs explain the types of general function qualifiers.

ADDRESS GENERAL FUNCTION QUALIFIER

The address general function qualifier, / A = (address), specifies an address that must be detected when the CPU function qualifier is satisfied to trigger a Break-point, Frame-Point, or External Trigger action. This function is disabled by the flag / AD.

DATA GENERAL FUNCTION QUALIFIER

The data general function qualifier, / D = (address), is data that is treated the same as the address general function qualifier above. This function is disabled by the flag / DD.

PROBE LOGIC STATE QUALIFIER

The logic state qualifiers (/PL, /PH, /DP) are states sensed by the Probe and are treated the same as the address and data general function qualifiers above. This function is disabled by the flag / DP. Activation on a high or low state is determined by the flags / PH or PL, respectively, on the same command line.

Table 4-8. General Function Qualifiers

COMMAND	DESCRIPTION
/A = (address)	Enable On (address)
/AD	Disable Address
/D = (data)	Trap On Specific Data
/DD	Disable Data
/PH	Trap On The High State Of Probe Signal
/PL	Trap On The Low State Of Probe Signal
/PD	Disable Trap On Probe State

LOOP COUNT QUALIFIER

A Loop Count qualifier, /L = (loops) can be appended to a Break-Point or Frame-Point command line.

NOTE

Enter the Loop Count in HEX format.

If appended to a Break-Point command, /L specifies the number of times the tester must detect a condition before a Break-Point occurs. If /L is appended to a Frame-Point command, it specifies the number of times a Frame-Point function is performed.

The loop count function is deactivated by sending a BP or FP command without a loop count qualifier included. Use of either "/L = 00" or "/L = 01" results in a Break-Point at the first occurrence of the condition or a single Frame-Point. The loop count function cannot be used with the External Trigger function.

CPU and General Function Qualifier Examples

Two examples using the Break-Point Function are as follows:

BP/RE/A=5A00

The command line translates into Break-Point on Read at address 5A00 Hex.

BP/OE/A=0A2E/PH/L=5

The command line translates into Break-Point on opcode fetch at address 0A2E Hex when the Probe is sensing a high state on the fifth loop with this condition.

Section 5
Maintenance

INTRODUCTION

This section provides user maintenance information for the Fluke 90. Included is a list of user replaceable parts, procedures for replacement of parts, and proper storage requirements during non-use of the tester.

Refer to Table 5-1 for part numbers needed for ordering new parts. Section 2 "UNPACKING THE TESTER" contains details for return shipment.

CLEANING

CAUTION

To avoid damaging the tester, do not use petroleum based solvents to clean the case, keys, or display window. These solutions will react with the plastics used in the tester.

Clean the case, keys, and display window with a damp cloth dipped in a mild detergent and water. Avoid allowing water to enter the case around the key edges.

REPLACEABLE PARTS

Table 5-1 contains the list of replaceable parts, the description of each part, and the Fluke part number.

Table 5-1. List of User Replaceable Parts

DESCRIPTION	FLUKE PART NUMBER
Microprocessor Clip	800110
Probe Assembly	825992
RS-232-C Cable	831776
Cable Adapter	831602

Components may be ordered from the manufacturer by using the manufacturer's part number, or from John Fluke Mfg. Co., Inc. or its authorized representative by using the Fluke part number.

In the event the part you order has been replaced by a new or improved part, the replacement will by accompanied by an explanatory note and installation instructions, if necessary.

To ensure prompt and efficient handling of your order, include the following information:

- Quantity
- Fluke Stock Number
- Description
- Instrument Model and Serial Number

Parts price information is available from the John Fluke Mfg. Co., Inc. or its representative. Prices are also available in the Fluke Replacement Parts Catalog, which is available on request.

TRANSPORT AND STORAGE REQUIREMENTS

The small size of the tester allows the tester to be carried in a tool box or briefcase. Avoid any vibration or temperatures outside those shown in Appendix B Specifications during transport.

NOTE

Do not pick up the tester using the cable as a handle. This may damage the cable or internal connectors.

Appendix A
Remote User Command Set

INTRODUCTION

The command syntax necessary to perform tests via the RS-232-C interface are listed in this Appendix. All commands require a ⟨CR⟩ (0D Hex) character for termination.

Some command sequences require optional data and/or required data. Optional data is shown in square brackets i.e., [address]. Required data is shown in parenthesis i.e., (baud). Required spaces are shown underlined "_". Multiple fields are shown by three periods i.e., [data]..[data] meaning multiple data values. All numbers are entered in Hexadecimal notation.

The "/L" flag included with the command sequence puts the command into a loop mode. The command is repeated over and over until a B (02 Hex) or ⟨ESC⟩ (1B HEX) character is sent to the tester, or the CLEAR or RESET key is depressed on the keypad.

CONTROL COMMANDS

Table A-1. Control Commands

COMMAND	HEX VALUE	FUNCTION	KEYPAD EQUIVALENT
^X	10	Step or Continue	ENTER
^Q	11	Resume Transmission (XON)	None
^S	13	Pause Transmission (XOFF)	None
^B or ⟨ESC⟩	02	Terminate Command	CLEAR

LOCAL/REMOTE COMMANDS

Table A-2. Local/Remote Commands

TEST	FUNCTION	SYNTAX
BUS TEST	Test Bus Ramp Test Shift Test	BT[/L] ⟨CR⟩ RT[/L] ⟨CR⟩ SH[/L] ⟨CR⟩
MEMORY TEST	Test Memory Checksum Test Memory Examine Memory Verify Memory Write Memory Soak Memory Fill	MT_(la)_(ha)[/L] ⟨CR⟩ CK_(la)_(ha)[/L] ⟨CR⟩ ME_(la)_(ha)[/L] ⟨CR⟩ MV_(la)_(d)_[d]...._[d][/L] ⟨CR⟩ MW_(la)_(d)_[d]...._[d][/L] ⟨CR⟩ MS_(la)_(ha)_(d)_(st)[/L] ⟨CR⟩ MF_(la)_(ha)_(d) ⟨CR⟩
I/O TEST	I/O Examine I/O Verify I/O Write	IX_(lp)_(hp)[/L] ⟨CR⟩ IV_(lp)_(d)_[d]...._[d][/L] ⟨CR⟩ IW_(lp)_(d)_[d]...._[d][/L] ⟨CR⟩
PROBE FUNCTIONS	QuickTrace Probe Address lines Probe Data Lines Probe Control Lines	QT PA PD PC

NOTES:

b = baud rate	(300, 600, 1200, 2400, 4800, or 9600)
d = data	(Hexadecimal number 00 to FF)
db = data bits	(7 or 8)
la = low address	four-digit, hexadecimal number 0000 to FFFF)
ha = high address	(A four-digit, hexadecimal number 0000 to FFFF)
m = message	(Alphanumeric entry less than 16 characters)
lp = low port address	(Two digit, hexadecimal number 00 to FF)
hp = high port address	(Two digit, hexadecimal number 00 to FF)
st = soak time	(A time in minutes between 0 and 255)

BREAK-POINT, FRAME-POINT, AND EXTERNAL TRIGGER COMMANDS

Table A-3. Break-Point, Frame-Point, and External Trigger Commands

COMMAND NAME	COMMAND LINE SYNTAX
Break-Point	BP(/cpu)[/gen]...[/gen]⟨CR⟩
Frame-Point	FP(/cpu)[/gen]...[/gen]⟨CR⟩
External Trigger	XT(/cpu)[/gen]...[/gen]⟨CR⟩
Disable BP, FP, XT	DB⟨CR⟩
Break-Point Status	BP*
Frame-Point Status	FP*
External Trigger Status	XT*

NOTES:

/cpu is a required CPU Function qualifier.
/gen is an optional General Function qualifier.
* without a CPU or General Function qualifier appended, BP, FP, and XT commands respond with a status condition.

CPU FUNCTION QUALIFIERS

Table A-4. CPU Function Qualifiers

COMMAND	DESCRIPTION
/RE	Enable BP, FP, or XT on Memory Read
/WE	Enable BP, FP, or XT on Memory Write
/IRE	Enable BP, FP, or XT on I/O Read
/IWE	Enable BP, FP, or XT on I/O Write
/OE	Enable BP, FP, or XT on OpCode Fetch
/IE	Enable BP, FP, or XT on Interrupt Acknowledge

GENERAL FUNCTION QUALIFIERS

Table A-5. General Function Qualifiers

COMMAND	DESCRIPTION
/A = (address)	Enable On (address)
/AD	Disable Address
/D = (data)	Trap On Specific Data
/DD	Disable Data
/PH	Trap On The High State Of Probe Signal
/PL	Trap On The Low State Of Probe Signal
/PD	Disable Trap On Probe State

MISCELLANEOUS REMOTE COMMANDS

Table A-6. Miscellaneous Remote Commands

COMMAND	DESCRIPTION
CP(_b)(_db)	Configure the RS-232-C interface
DN[/M]	Down-load to the UUT
UP(_la)(_ha)[/M]	Up-load from the UUT
RH[/L]	Reset UUT
T1(_m)	Display message
T2(_m)	Display message
EC	Enable keypad intercept

Appendix B
Specifications

ENVIRONMENTAL SPECIFICATIONS

Relative Humidity

Up to 80%	0 to 35°C
Up to 70%	35 to 50°C (non-condensing)

Ambient Temperature	0 to 50°C
Mechanical Shock and Vibration	MIL-T-28800D Class 3

Storage Conditions

Ambient Temperature	-40 to 70°C
Relative Humidity	5 to 95%

GENERAL SPECIFICATIONS

Dimensions	11 inches (279.4 mm) x 6 inches (152.4 mm) x 3 inches (76.2 mm) (without feet)
Weight	2.25 lbs (1020.58 g)

POWER

Operating Voltage

From UUT	4.35V dc to 6.3V dc
From External Power Supply	7V dc to 12V dc

Power Consumption	Less than .75 watts
Common Mode (Maximum Interface Voltage)	30V
SAFETY	Meets ANSI/UL 478 and IEC 348 standards.

Appendix C
Sales and Service Centers

U.S. SALES AREAS for all Fluke products

Alabama

Huntsville
4920 Corporate Drive
Suite J
Huntsville, AL 35805-6202
(205) 837-0581

Arizona

Tempe
2211 S. 48th Street
Suite B
Tempe, AZ 85282
(602) 438-8314

Tucson
(602) 790-9881

California

Burbank
2020 N. Lincoln Street
Burbank, CA 91504
(213) 849-7181

Northern
2300 Walsh Ave., Bldg. K
Santa Clara, CA 95051
(408) 727-0513

San Diego
(619) 292-7657

Southern
P.O. Box 19676
Irvine, CA 92713-9676
16969 Von Karman
Suite 100
Irvine, CA 92714
(714) 863-9031

Colorado

Denver
14180 E. Evans Ave.
Aurora, CO 80014
(303) 695-1000

Connecticut

Hartford
Glen Lochen East
41-C New London Turnpike
Glastonbury, CT 06033
(203) 659-3541

Florida

Clearwater
(813) 799-0087

Miami
(305) 462-1380

Orlando
940 N. Fern Creek Ave.
Orlando, FL 32803
(305) 896-4881

Tampa
(813) 251-9211

Georgia

Atlanta
2700 Delk Road
Suite 150
Marietta, GA 30067
(404) 953-4747

Illinois

Chicago
1150 W. Euclid Avenue
Palatine, IL 60067
(312) 705-0500

Indiana

Indianapolis
8777 Purdue Road
Suite 101
Indianapolis, IN 46268
(317) 875-7870

Louisiana

New Orleans
(504) 455-0814

Massachusetts

Boston
Middlesex Technology Center
900 Middlesex Turnpike
Building 8
Billerica, MA 01821
(617) 663-2400

Maryland

Baltimore
(301) 792-7060

Rockville
5640 Fishers Lane
Rockville, MD 20852
(301) 770-1570

Michigan

Detroit
33031 Schoolcraft
Livonia, MI 48150
(313) 522-9140

Minnesota

Bloomington
1801 E. 79th St.
Suite 9
Bloomington, MN 55420
(612) 854-5526

Missouri

St. Louis
11756 Borman Drive
Suite 160
St. Louis, MO 63146
(314) 993-3805

North Carolina

Greensboro
1310 Beaman Place
Greensboro, NC 27408
(919) 273-1918

New Jersey

Paramus
P.O. Box 930
Paramus, NJ 07653-0930
West 75 Century Road
Paramus, NJ 07652
(201) 262-9550

New Mexico

Albuquerque
(505) 881-3550

New York

Rochester
4515 Culver Road
Rochester, NY 14622
(716) 323-1400

Ohio

Cleveland
Plaza South Three
Suite 402
7271 Engle Road
Middleburg Heights, OH 44130
(216) 234-4540

Oklahoma

Northeast
(405) 236-2977

Oregon

Portland
(503) 227-2042

Pennsylvania

Malvern
200 Lindenwood Drive
Malvern, PA 19355
(215) 647-9550

Pittsburgh
(412) 261-5171

Texas

Austin
(512) 459-3344

Dallas
1801 Royal Lane
Suite 307
Dallas, TX 75229
(214) 869-0311

El Paso
(915) 533-3508

Houston
(713) 240-5995

San Antonio
10417 Gulfdale
San Antonio, TX 78216
(512) 340-0498

Utah

Salt Lake City
(801) 268-9331

Washington

Seattle
5020 148th Ave. N.E.
Suite 110
Redmond, WA 98052
(206) 881-6966

Washington, DC

Washington, DC
(301) 770-1570

INTERNATIONAL SALES OFFICES

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(For Philips products)
24 rue Bougainville
El Mouradia, Alger
Tel: 60 14 05
TLX: 62221

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Phillps Antillana N.V.
(For Philips products)
Schottegatweg Oost 146
P.O.Box 3523
Willemstad, Curacao
Tel: 599-9-615277
TLX: 1047

Argentina
Coasln S.A.
(For Fluke products)
Virrey del Pino 4071DPTO E-65
1430 CAP FED
Buenos Aires, Argentina
Tel: (54) (1) 552-5248
TLX: (390) 22284

Philips Argentina S.A.
(For Philips products)
Casilla Correo 3479
Vedia 3892
1430 Buenos Aires
Tel: 54-1-5414106/5417141
TLX: 21359/21243

Australia
Elmeasco Instruments Pty, Ltd.
(For Fluke products)
P.O. Box 30
Concord, N.S.W. 2137
Australia
Tel: (61) (2) 736-2888
TLX: (790) AA25887
FAX: (61) 2-733663

Elmeasco Instruments Pty, Ltd.
(For Fluke products)
P.O. Box 623
12 Maroondah Highway
Ringwood, Victoria 3134
Australia
Tel: (61) (3) 879-2322
TLX: (790) AA30418
FAX: (61) 3-879-4310

Elmeasco Instruments Pty, Ltd.
(For Fluke products)
P.O. Box 274
Salisbury, Qld Australia 4107
Tel: (61) (7) 875-1444
TLX: (790) AA44062

Elmeasco Instruments Pty, Ltd.
(For Fluke products)
P.O. Box 154
Prospect, South Australia 5082
Tel: (61) (8) 344-9000

Elmeasco Instruments Pty, Ltd.
(For Fluke products)
32 Teddington Rd.
Victoria Park
Western Australia 6100
Tel: (61) 9-470-1855

Phillps Scientific & Industrial Equipment Division
(For Philips products)
Centrecourt 25-27 Paul Street
North Ryde
Sydney N.S.W. 2113
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